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FPGA IMPLEMENTATION OF LOW POWER SRAM BASED PROCESSOR IN 8T USING HETTs

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Abstract— In MOSFETs lower limit sub threshold swing (60mv/decade) restricts the low power operation. Low voltage operation is enabled by low V_{th} while maintaining performance. Hence steep sub threshold slopes provide power-efficient operation without any loss of performance. To obtain sub threshold swings of less than 30mV/decade with large ON current, Si/SiGe heterojunction tunneling transistor uses gate controlled modulation. To overcome the impact of HETT characteristics on SRAM, seven transistors HETT based SRAM design is introduced. Compared to CMOS this new 8T HETT SRAM achieves reduction in leakage power.

Keywords-8T SRAM, low-power, heterojunction tunneling transistors(HETT), tunneling transistor.

I. INTRODUCTION

Low-power design technique is the most effective operation for its quadratic dynamic energy saving. The theoretical lower limit of sub-threshold swing in MOSFETs (60 mV/decade) significantly restricts low-voltage operation since it results in a low ON-to-OFF current ratio at low supply voltages. In low power techniques, low voltage operation is the effective low-power design techniques because of its quadratic dynamic energy saving. Low- power circuits based on new Si/SiGe heterojunction tunneling transistors (HETTs) that have a sub-threshold swing of <60 mV/decade.8T shall produce a better power consumption comparing to other T cells.

II. RELATED WORKS

2.1. HETTS CHARACTERISTICS

A heterojunction is the interface that occurs between two layers or regions of dissimilar crystalline semi-conductors. heterojunction transistors are fully compatible. The differences between HETTs and traditional MOSFETs must be considered. HETTs display asymmetric conductance. The source and gate are interchangeable in MOSFETs and determined by the voltages during the operation. However in HETTs, source and drain are determined at the time of fabrication.

Tunneling transistors have some slope limitation due to thermionic nature of conventional MOSFETs, since there is a turn-on it cannot be governed its emission over a barrier. Asymmetric current flow is taking as an advantage. Compared to CMOS this new HETT SRAM achieves 7-37 times reduction in leakage power. The ON current drops dramatically because of the lack of gate overdrive, resulting in large transition delays at low supply voltages. The threshold voltage can be reduced to regain this performance loss. But it exponentially increases the OFF current, which leads to problems in applications that spend significant time in the standby mode. There have been new devices with steeper sub threshold slopes then traditional MOSFETs. While maintaining low leakage, steep sub threshold slope enables operation with a much lower threshold voltage.

2.2. AN ULTRA-LOW-ENERGY MULTI-STANDARD CMOS WITH Vth

Static random access memory (SRAM) is an indispensable part of most modern VLSI designs and dominates silicon area in many applications. In scaled technologies, maintaining high SRAM yield becomes more challenging, At the same time, low power design is a key focus throughout the semiconductor industry. Since low voltage operation is one of the most effective ways to reduce power consumption due to its quadratic relationship to energy savings, lowering the minimum operating voltage (V_{min}) of SRAM has gained significant interest.

The concept is about presenting a design technique for sub-threshold operation to achieve low energy dissipation that is suitable for digital consumer electronic applications. They possess some demerits in which ultra-low voltage processor is used for less power during performance. The technique that enables one network to send data via another network where the SRAM cell topology was presented with 7 – 37 x leakage power reduction.

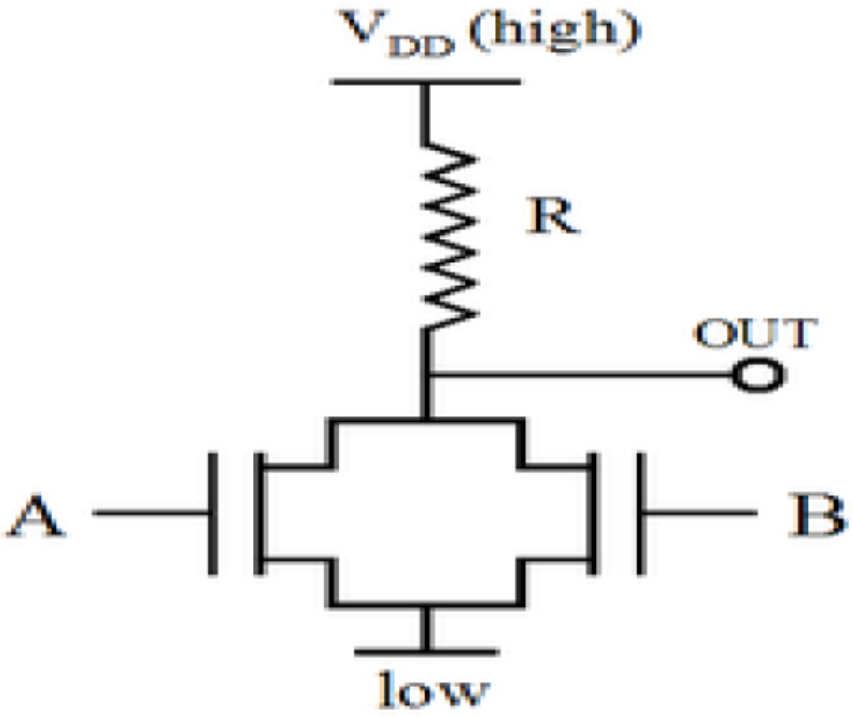

Figure 2. Full Down Network

2.3. VARIATION-AWARE STATIC AND DYNAMIC WRITABILITY ANALYSIS IN 8-T SRAMS

To mitigate variability and reduce V_{min}, it is important to understand SRAM failure modes and quantify immunity to failures. To ensure robust operation at low voltage in nano scale technologies, 8-T bit-cell has been proposed which can be separately optimized for read and write since bit-cells are not interleaved. However, when 8-T bit-cells are interleaved for immunity to soft errors, half select disturb issue arises and it limits the freedom to maximize its writability. In terms of dynamic writability, the longer pulse width is favorable to write operation while the shorter pulse width is favorable to immunity to half select disturb.

As process technology scales, SRAM robustness is compromised. In addition, lowering the supply voltage to reduce power consumption further reduces the read and write margins. To maintain robustness, a new bit cell topology, 8-T bit cell, has been proposed and read where write operation

can be separately optimized.. The half select disturb issue limits the use of a bit-interleaved array configuration required for immunity to soft errors. The opposing characteristic between write operation and half select disturb generates a new constraint which should be carefully considered for robust operation of voltage-scaled bit-interleaved 8-T SRAMs. Bit-interleaved writability analysis that captures the double-sided constraints placed on the word-line pulse width and voltage level to ensure writability while avoiding half select disturb issue.

The concept is about lowering the supply voltage to reduce the power consumption further it reduces the read and write margins. A new bit-cell topology has been introduced in-order to maintain robustness. The drawback is that when voltage lowers then power also gets lowered where it further reduces read and write margins. The high- word boosting does not guarantee better robustness as it lowers half select immunity in which it's a major drawback due to word-line and the reduction in power will be as in other bit-cells. The static 8T level perform with half select process.

2.4. COMPLEX FFT CORE WITH SUPERPIPELINING

Aggressive voltage scaling has been shown to be an important technique in achieving highly energy efficient circuits. Specifically, scaling Vdd to near or sub-threshold regions has been proposed for energy-constrained sensor systems to enable long lifetime and small system volume. However, voltage scaling has several limitations, including significant performance degradation and heightened delay variability due to large Id sensitivity to variations in the ultra-low voltage (ULV) regime. In addition, energy efficiency degrades below a certain voltage, Vmin, due to rapidly increasing leakage energy consumption.

Pipelining is a well-known method to improve performance, typically at the expense of energy consumption due to added sequential elements. Make the observation that inserting additional pipeline latches improves both energy efficiency and performance in the ULV operating regime. Since pipelining shortens the clock period, it limits leakage energy consumed by idling gates, which reduces energy consumption and allows further voltage scaling.

In case of pipelining the clocking overhead is reduced hence super pipelining is used to address the latch-based design. The concept is based on using the circuit and architectural methods to reduce the minimum energy point while simultaneously improve performance and robustness. By inserting additional pipeline latches it improves both energy and efficiency and performance in ULV operating regime.

2.5. PROSPECT OF TUNNELING GREEN TRANSISTOR

Reducing the voltage V_{dd} is a powerful way to reduce IC energy consumption, which is proportional to Vdd2. Power usage was kept under control when V_{dd} was reduced in proportion to half-pitch up to 130nm . The 14nm node is projected to operate at 0.7V, making the power consumption 25x larger than it would be if operated at 0.14V as the past trend suggests. While IC power consumption has been much discussed as a thermal management challenge, it is also responsible for a few percent of the electricity usage and growing fast. A low voltage transistor (Green Transistor, gFET) is needed.

III. METHODOLOGY AND MATERIALS USED

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations in addition to such six-transistors. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell.

This improves SRAM bandwidth compared to DRAMs in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bit line to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable. These access the SRAM band-with with the other cell- topology and better result could be obtained.

IV. SRAM OPERATIONS

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

(i) *Standby* -If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

(ii) Reading -Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by pre charging both the bit lines to a logical **1**, then asserting the word line WL, enabling both the access transistors.

(iii) Writing -During a read operation these two bit lines are connected to the sense amplifier that recognizes if a logic data ―1‖ or ―0‖ is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is connected to the output pad.

4.1. CMOS STANDARD 6T SRAM

SRAM cell is composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors connected to the row line. This configuration is called a 6T Cell. The main disadvantage of this cell is its large size. To understand the difference between HETT-based 6T SRAM and CMOS-based 6T SRAM, trace the current flow paths in read and write operations.

4.2. 6T SRAM DESIGN WITH HETT

The asymmetric current flow of HETT places restrictions on the use of the pass gate and the transmission gate. This limitation is not severe for logic circuits since the CMOS logic, which is the most widely used logic, is not affected by this property because the current is expected to flow only in one direction in the channel of each transistors. Moreover, any pass-gate logic can be easily converted to CMOS logic to prevent malfunctions with HETT. The asymmetric current flow does not have a proper current flow through the unit and it can be able to produce a better area and power consumption in other topology.

4.3. 7TRANSISTOR SRAM

A seven-transistor SRAM cell intended for the advanced microprocessor. A low power write scheme, which reduces SRAM power by using seven-transistor sense-amplifying memory cell, has been described. By reducing the bit-line swing and amplifying the voltage swing by a sense amplifier, which is a part of the memory cell, the charging and discharging component bit / data lines power consumption is reduced. A comparison can done between existing six-transistor technology and the proposed (seven-transistor) technology.

4.4. 7T SRAM for HETT

In 7T topology, readability/write-ability tradeoffs in HETT-based 6T SRAM are overcome by utilizing separate read and write structures. The reduced 8T read enables extremely robust read with minimal additional number of HETT, and two-side NHETT pull-down write enables robust write with cell β -ratio of 1, where all HETT sizes can be minimum.

4.5. 7T HETT SRAM IN REGISTER FILES OF PROCESSOR

To obtain the power reduction in processor, the predesigned 7T HETT SRAM is used in the register files of the processor. Here SRAM and CAM based processors are used. CAM based processors are used to get the address of the specified date or input. Register files and data path are used to gain insight into the internal logic for data movement between registers in a computer. RAMs are distinguished by having dedicated read and write ports, whereas ordinary multi-ported SRAMs will usually read and write through the same ports.

Tanner EDA provides of a complete line of software solutions for the design, layout and verification of analog and mixed-signal (A/MS) ICs and MEMS. Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. A low learning curve, high interoperability, and a powerful user interface improve design team productivity and enable a low total cost of ownership (TCO). Capability and performance are matched by low support requirements and high support capability as well as an ecosystem of partners that bring advanced capabilities to A/MS designs. Tanner Tools v16 offers many new features and significantly greater functionality. The 8T SRAM performance will be better compared to other SRAM and Power savings can be done through HETTs as in other SRAM cell topology.

V. CONCLUSION

Power minimization has become a primary concern in microprocessor design. In recent years, many circuit and micro-architectural innovations have been proposed to reduce power in many individual processor units. The main advantages of 8T SRAM HETT are <15% area overhead ,improved robustness, low leakage current, compatible fabrication process, separate current paths for read and write operation and significantly reduced standby power as compared to that of CMOS 6T SRAM and 7T SRAM. These static access can be performed and obtained a better result using TANNER EDA tool in 8T. Power comparison will be better compared to other previous SRAM transistors.

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