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Design of Low Power Modified Wilson Current Mirror Based Level Shifter using Forced PMOS Method

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Abstract — Wide range level shifters are a fast energy efficient converter capable of converting low voltage to high voltage. Level Shifters are used to shift the voltage from one level to another level. Multi voltage system utilizes the advantage of level shifter. Multi voltage systems consist of low voltage as well as high voltage. Existing method was implemented by using LVT (Low Threshold Voltage Transistor) which produce the leakage power dissipation. Proposed method is implemented by using the Forced PMOS method to reduce the leakage power. Usually LS are inserted only while crossing low voltage domain to high voltage domain. In this paper modified Wilson current mirror based level shifter is designed by using stack technique. Measurement results were demonstrated using Mentor Graphics.

Keywords — Level Shifter, Multi voltage system, Forced PMOS techniques

I. INTRODUCTION

The growing market of mobile, battery- powered electronic systems (e.g., cellular phones, personal digital assistants, etc.) Demands the design of microelectronic circuits with low power dissipation. More generally, as density, size, and complexity of the chips continue to increases, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. In the past ten years, several techniques, methodologies and tools for designing low power circuits have been presented. However, only a few of them have found their way in current design flows [1].There are three major sources of power dissipation n in a CMOS circuit. Those are switching power, short circuit power and leakage power. Switching power is due to the charging and discharging capacitors driven by the circuit. Short circuit power is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously. Finally, Leakage power is originates from substrate injection and sub threshold effects. One of the main reasons causing the leakage power increase is the increase of sub threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub threshold leakage power increase exponentially as threshold voltage decreases. Stack method, Forced NMOS, Forced PMOS and sleepy keeper method are the some of the leakage current reduction methods [2].

1.1. LEVEL SHIFTERS

A. Conventional Level Shifter

Sub threshold LSs are surveyed in this section. Conventional cross-coupled LS is a differential cascade voltage switch logic (DCVSL) for raising a low voltage level, as shown in figure.1. The drive strength of NMOS transistors is enhanced to overcome the leakage of weakly conducting PMOS transistors. The operating range of CC LSs depends on the transistor threshold voltage (v_t) and size; however, the operating range of CC LSs is difficult to extend to the sub threshold region (with respect to the NMOS v_t) because the NMOS drive strength decreases exponentially. For converting a sub threshold voltage, CC LS require an exponential increase in NMOS transistor size, which is impractical [3].

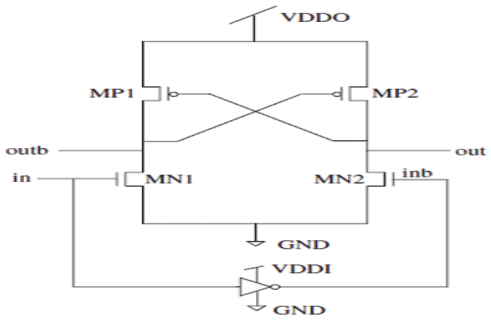

Figure.1.Conventional Level Shifter

B. Current Mirror based Level Shifter

Figure .2 shows conventional LS that uses a basic current mirror (CM).The conventional CM LS can convert a deep sub threshold level because a high drain-to-source voltage of PMOS transistors facilitates the construction of a stable current mirror, which offers an effective on-off current comparison at the output node. However, a high amount of Quiescent current occurs when the input voltage is super threshold. This high power consumption limits the use of the conventional CM LS [4].

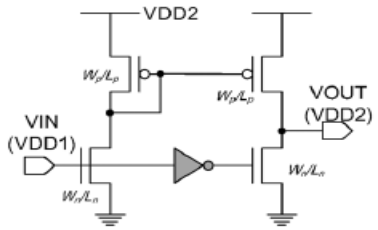

Figure .2. Current Mirror Based Level Shifter

C. Wilson Current Mirror Based Level Shifter

Figure .3 shows a CM-type LS that uses a Wilson current mirror (WCM), which clamps the quiescent power consumption under a super threshold input [4].

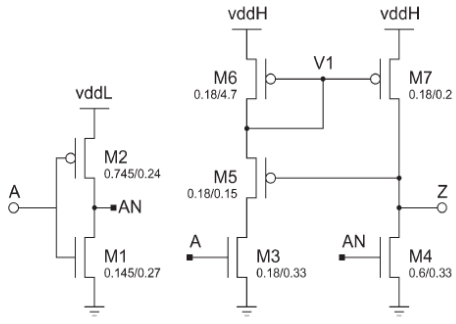

Figure .3. Wilson Current Mirror based level shifter

In [5] shows a two-stage CC LS (TSCC), of which the pull-up driving strength is reduced by a header NMOS, which expands the convertible input voltage. In [6] shows a CC-type LS (CCPNR), in which the output stage is a part of the NOR gate fed by the primary input to accelerate the overall LS speed. I n [7] uses a logic Error Correction Circuit (LECC), which monitors input and output updates data during the pulse. The MWCMHB LS is a hybrid structure comprising a modified Wilson current mirror and CMOS logic gates [8].The input and output levels range from a sub

threshold voltage to the standard supply voltage defined in a transistor technology. Bidirectional level conversion is available; that is, input and output levels can be scaled independently.

D. Modified Wilson Current Mirror Based Level Shifter

The MWCMHB LS structure is illustrated with three circuit blocks, as shown in Figure .4. A modified Wilson current mirror (MWCM) is located in Block 1. When VDD1 is sub threshold and VDD2 is high, the MWCM structure balances the rising and falling delay at Node A, without losing the original static bias that is favored in the WCM LS [4].However, when the VDD1 and VDD2 levels are close, the MWCM encounters the same problem as the WCM does. The cascode PMOS has insufficient drive currents and increases the rising delay. Therefore, in Block 3, a delay path is designed adaptively to reduce the rising delay and maintain a moderate duty cycle. An output inverter offers sufficient drive strength, which is required in a standard cell design. Unlike the CCPNR LS [6], which has a similar structure, the proposed LS uses a CM-type amplifier, a balancing delay path, and a complementary OR gate in Block 2.The CM type structure provides a wide operating range, and the stacked PMOS transistor in the complementary OR gate limit the leakage current.

Level shifter should satisfies the following condition those are

1. Small area for sub threshold level conversion
2. Low power consumption in super threshold Operations
3. Balancing rising and falling delay in the operating Range
4. Bidirectional level conversion

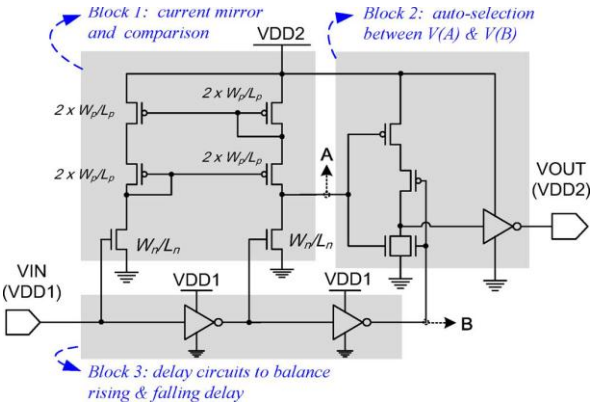

Figure.4. Modified Wison Current Mirror based Level Shifter

II. POWER REDUCTION METHOD

Forced PMOS is one of the method of leakage power reduction Technique. In this method pull down network is not modified. Pull up network is only modified by the Forced PMOS method. An Existing PMOS Transistor is split into two each transistor is having the W/L ratio of half compare with existing transistor. Consider inverter as an example. By applying this Forced PMOS method to the inverter the power can be decreased from 2 pW to 1.75 pW.In this method two PMOS transistor increases the delay in the current flow path so that power can be increased. Other leakage power reduction methods are stack method and forced NMOS method.

Stack approach is one of the leakage power reduction methods, which forces a stack effect by breaking down an existing transistor into two half size transistors [9]. When the two transistors are turned off together, induced reverse bias between the two transistors results in leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach [10].

In forced NMOS approach if input is given low as compared to threshold voltage., then at the same time PMOS turns on and NMOS turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time PMOS turns off and NMOS turn on. Here, the two NMOS transistors which increases the delay in the flow of the current which ultimately decreases the leakage power in the circuit [11].

III. PROPOSED LEVEL SHIFTERS

In this section Existing Level shifters are modified by using the Forced NMOS approach. Figure 5,6,7,8 shows the conventional cross coupled, Current mirror based level shifter, Wilson current mirror based level shifter and modified Wilson current mirror based level shifter. These level shifters were designed by using the Forced PMOS method. Power was reduced when comparing with existing level shifters.

In forced PMOS method pull up network is only modified. Here existing PMOS transistor W/L ratio is 0.5u/0.3u proposed circuit was designed by splitting the existing PMOS transistor into two each having the W/L ratio of 0.42u/0.5u.

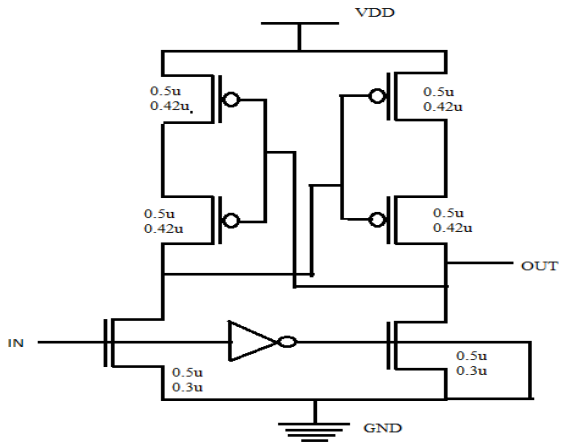

Figure .5. Modified Conventional cross coupled level shifter

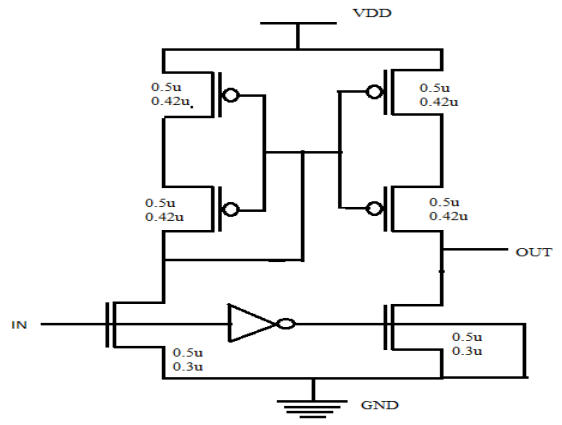

Figure .6. Current mirror based level shifter using Forced PMOS

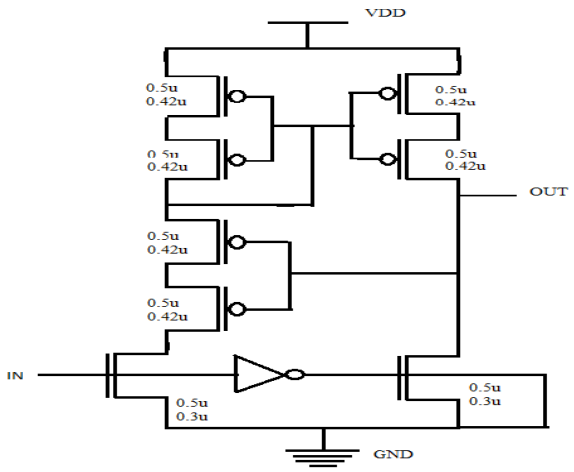

Figure.7. Wilson Current Mirror based level shifter using Forced PMOS

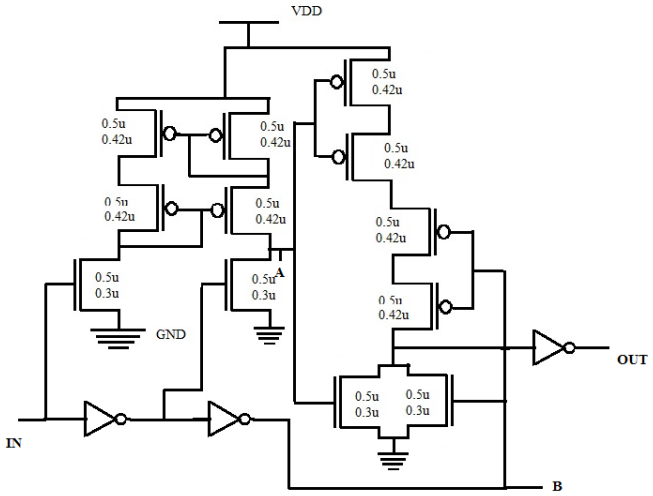

Figure.8. MWCM based level shifter using Forced PMOS

IV. SIMULTION AND RESULT

Simulation results for Proposed Level shifters are shown in Figure 9,10,11,12 respectively. Waveform for Modified Conventional cross coupled level shifter is shown below diagram. Input voltage for cross coupled voltage is 2.5v and output voltage is 0.22v. Current mirror based level shifter is also shift the voltage from 2.5v to 0.22v.

Wilson current mirror based level shifter is used to shift the voltage from 2.5v to 0.13v.Modified Wilson current mirror based level shifter is a bidirectional level shifter which is used to shift the voltage from 1v to 5v.Waveform for MWCM is shown in Figure 12.

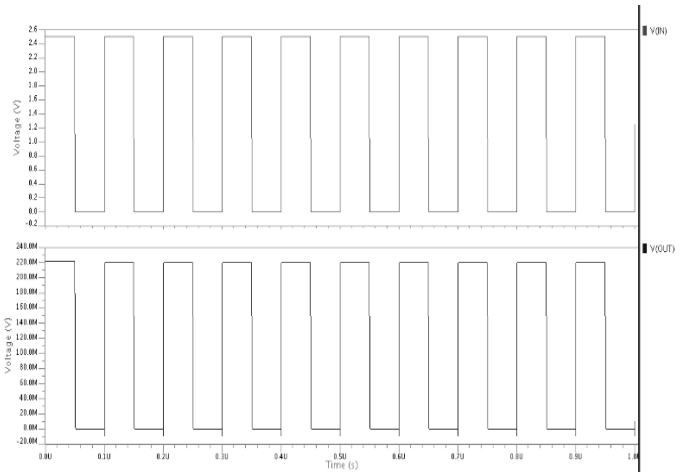

Figure.9. Waveform for conventional level shifter

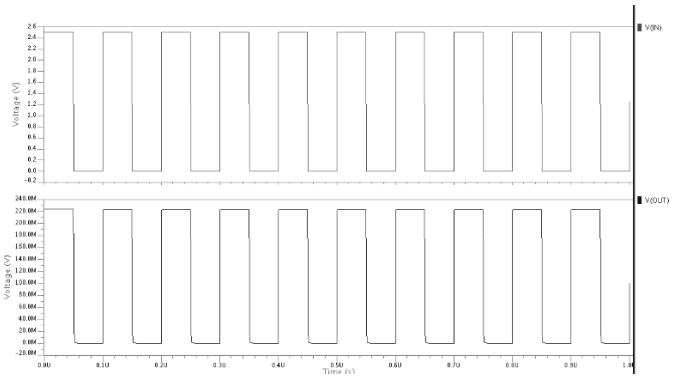

Figure .10. Waveform for current mirror based level shifter

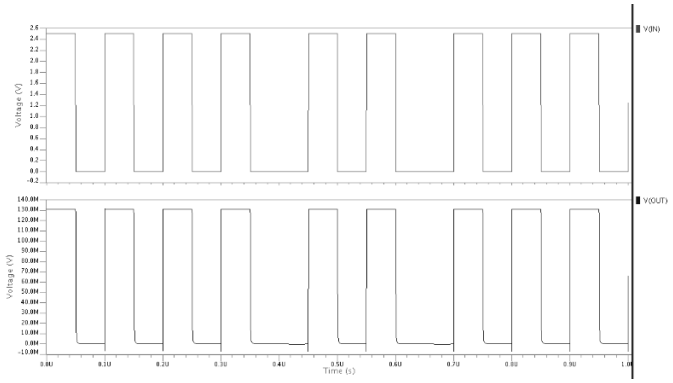

Figure .11. Waveform for Wilson current mirror based level shifter

Simulation can be performed by using the Mentor Graphics. Mentor Graphics is one of the Electron Device Automation tool.

In this tool Eldo, Calibre are mainly used for the simulation, LVS and DVS check. This Software is run at the LINUX operating system.

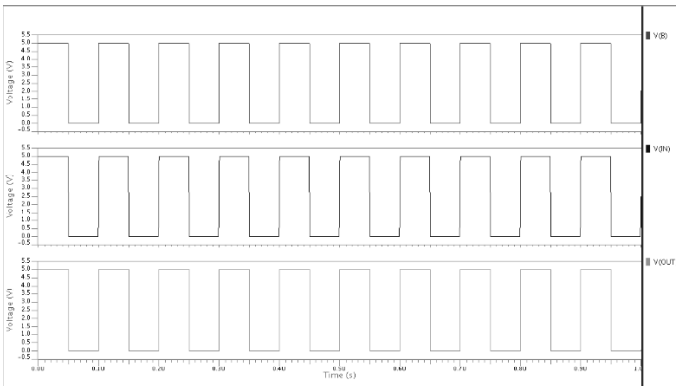

Figure .12. MWCM based level shifter

Table. 1. Power and delay for various level shifter without forced PMOS method

Level shifters	Power	Delay
Conventional Level Shifter	4.6923(mW)	0.1 ns
Current mirror based level shifter	4.3694(mW)	0.2ns
Wilson current mirror based level shifter	1.7154(mW))	0.1ns
Modified Wilson current mirror based level shifter	250.7207(nW)	0.3ns

Table. 2. Power and delay for various level shifter with forced PMOS method

Level shifters	Power	Delay
Conventional Level Shifter	1.8021(mW)	0.3 ns
Current mirror based level shifter	1.7876(mW)	0.5ns
Wilson current mirror based level shifter	1.0391(mW)	0.2ns
Modified Wilson current mirror based level shifter	250.0337(nW)	0.5ns

Table 1 and 2 shows the comparison of Normal level shifter design and level shifter design using Forced PMOS method. Comparing with existing and proposed method delay is slightly increased and power is decreased in proposed method.

V. CONCLUSION

Conventional level shifter has the power dissipation of 4.6943 mW. The same circuit is designed by using Forced PMOS method means that time power is decreased from 4.6943mW to 1.8021mW.Likewise Current mirror based level shifter, Wilson current mirror based level shifter, Modified Wilson current mirror based level shifter is reduce the power consumption from 4.3694mW,1.7154mW and 250.7207nW to 1.7876mW,1.0391mW and 250.0347nW.

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