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QUANTUM DOT CELLULAR AUTOMATA BINARY COMPARATOR USING REVERSIBLE GATE

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Abstract: - Quantum dot cellular automata (QCA) is one of the few alternative computing platform, has the potential to be a promising technology due to high speed, small size, and low power consumption in comparison with CMOS technology. The proposed comparator is designed and simulated using QCA designer tool. Two different comparator are designed to exhibit higher performance and to reduced the overall area. The binary comparator is designed to reduced the area, majority cell and power. Here reversible gates [Feynman gate] are used to reduced the energy losses and information losses.

Index terms: - Quantum dot cellular automata (QCA), binary comparator, majority gates, reversible gates.

I. INTRODUCTION

Nanotechnology is a promising future for designing QCA .It takes great advantage of a physical effect that the coulomb force that interacts between electrons. In CMOS technology there is physical limits to reduced the area transistor sizing etc, to overcome the problem QCA are designed not operated by which consists of few square nanometers. By using the quadric cells the QCA are implemented. The cell consists of four potential wells which locate at the corner of the QCA cell.

QCA provides a new method of computation and information transformation. In QCA, binary information is encoded by the configuration of electrical charges in a QCA cell. Computation is realized via the Columbic interaction between neighboring cells. Because of the Columbic nature of quantum cells, current does not flow between cells.

Moreover, power dissipation in QCA circuits is ultra low compared with conventional CMOS circuits

The electrons are used to store and transmit the data. These electrons are transmit through tunneling junction. Due to the repelling force the electrons moves to opposites corners of the quantum cell, resulting in two possible arrangements representing binary 0 and 1.A QCA design are partitioned the clock zones that are progressively associated with four clock signals, each phase shifted by 90deg.

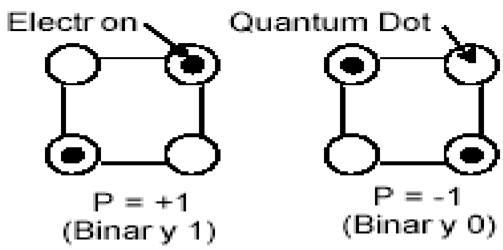


Fig.1. QCA cell.

Limits of cmos Technology Scaling and Technologies the cmos ciruits have the diadvantage, to overcome the problem nanometer square Quantum dot cellular automta are implemented. In this QCA designer several arithmetic ciruits such as adder.multipliers and comparators are proposed. The state of a cell can also be transferred to multiple neighboring cells.This allow us to build "wires" made of QCA cell, to transport information over larger distances.

II. INFORMATION AND DATA PROPAGATION.

If two QCA are placed near to each other it is possible to exchange their state i.e the adjustment of electrons in them. The QCA cell that should transfer its state to a neighboring cell must have its tunnel junctions closed, the tunnel junctions in the neighboring cell have to be open, to allow the electrons to travel through the tunnel junctions between the potential wells. As soon as they open, the electrons in the neighboring cell are pushed by the Coulomb force of the original cell as far away as possible. As they also are pushed away from each other, they will travel into the same potential wells as in the original cell. As soon as the tunnel junctions are closed again, the transfer of the state is completed.

Boolean algebra based on a geometrical interpretation of three-variable Boolean functions to facilitate the conversion of sum-of products expressions into reduced majority logic. The fundamental QCA logic primitives are the three input majority gate ,wire, and inverter. Each of these can be considered as a separate QCA locally interconnected structure, where QCA digital architectures are combination of these cellular automata structures. These two arrangements are denoted as cell polarization p=+1and p=-1[5].By using cell polarization to represent logic"1" and to represent logic"0" binary information is encoded in the charge configuration of the QCA cell.

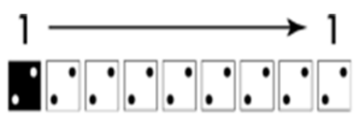


Fig.2. QCA wire

The majority gate itself contains only to electrons and perform the logic function that would take many transistor to accomplish.[5][6].

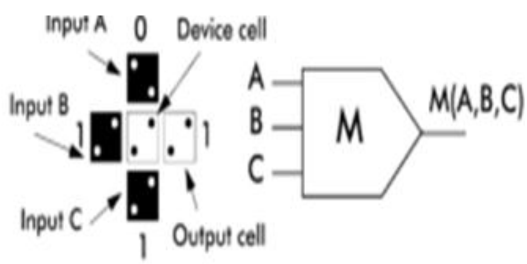


Fig.3.majority gate

The linear array thus act as binary wire ,transmitting information from the drive end to the unconstrained end. The wire function well so long as the energetic of the coulomb interaction dominated the kinetic action which tend to cause the two electron wave function to spread[5] [6].The bistability of each cell in the wire also resulted in an insensitivity to geometrical variation and that would take many transistors to accomplish.

III. REVERSIBLE GATES

By using reversible gates the energy losses are reduced. Reversible gates are used to o reduce heat dissipation.

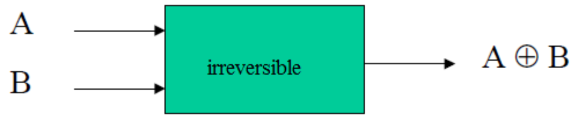


Fig.4. irreversible gate

The irreversible gates are dissipate large amout of energy losses. In order to avoid the losses the reversible gates are designed.

Information loss=energy loss.

Reversible logic structure requires an identical number of input and output lines.

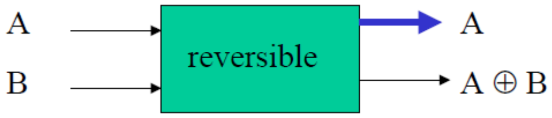


Fig.5. reversible gate

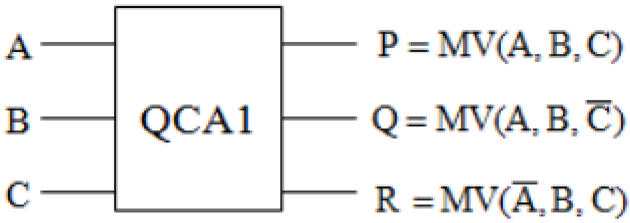


Fig.6. QCA1 reversible gate

QCA1reversible gate are suitable for the majority gate for QCA computing. Here (A,B,C) are mapped to (P,Q,R)[7].

A	B	C		P	Q	R
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	1
0	1	1		1	0	1
1	0	0		0	1	0
1	0	1		1	0	0
1	1	0		1	1	0
1	1	1		1	1	1

Table.1. Truth table for QCA1[7]

IV. BACKGROUND WORK

Datapath components in modern high performance superscalar processors employ a significant amount ofassociative addressing logic based on the use of comparatorsthat dissipate energy on a mismatch. In order to avoid the mismatch the design of comparator using microprocessor is designed. Their performance level is high but it consists of five metal layers. Hence it dissipate large amount of power. The design of two new comparator circuits that is predominantly dissipate energy on a match, thus resulting in very significant savings incomparator power dissipation.

The logic structure and interconnection in the QCA cell are designed either in coplanar cross or bridge technique. QCA technology is the inverter and the majority gate (MG).These majority gates are performs with same clock signal.

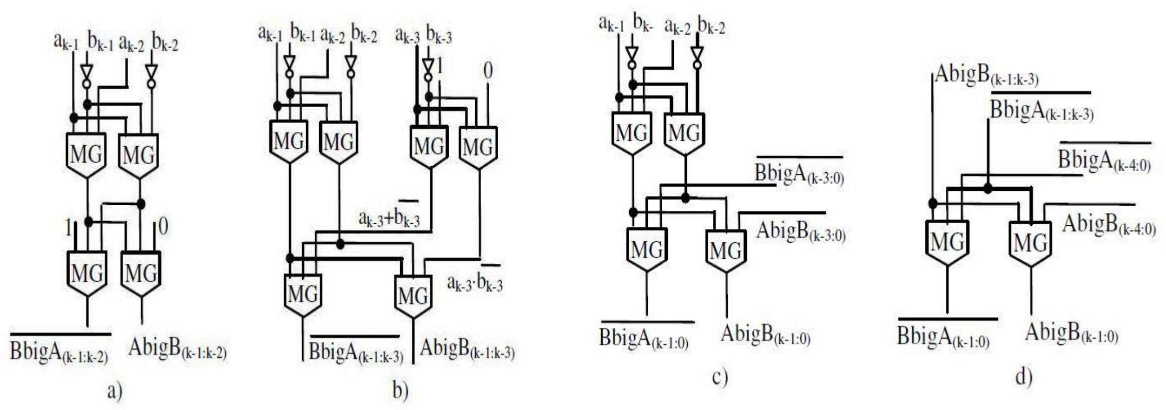
$$M(a,b,c)=a.b+a.c+b.c$$

A 1-bit binary comparator recevies two bita a and b and it compare whether a and b are equal,or greater than each other,or less than each other.This comparator is slow and it take large amount of power to yield the output.To overcome this problem a tree based architecture are exhibited to achieve high speed.The inputs are given to the majority gates which proceed through the proper number of cascaded in which OR,AND gates are implemented.In the tree based architecture the delay will increse according to the n bit comparator.

V. ARCHITECTURE

QCA modules have been used to design two different structures of full comparators here named cascade- and tree-based architectures.

However, many other structures can be designed by combining the basic modules in different manners.



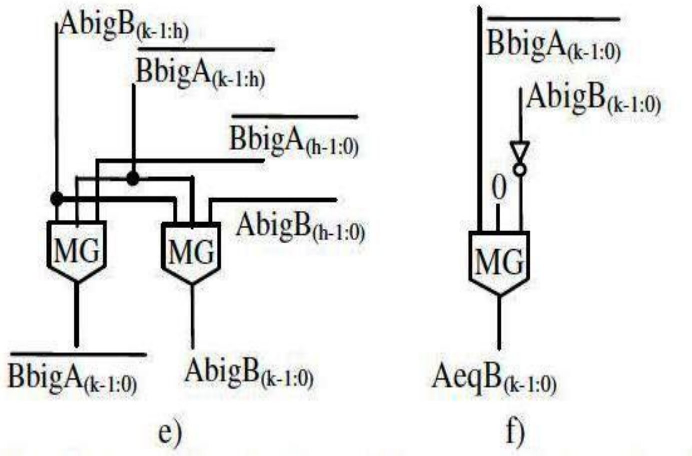
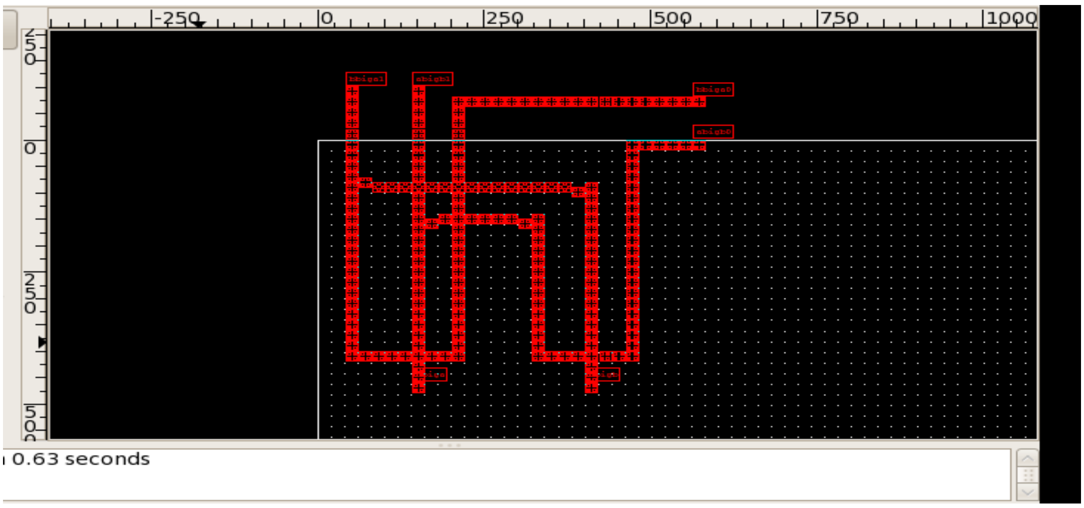
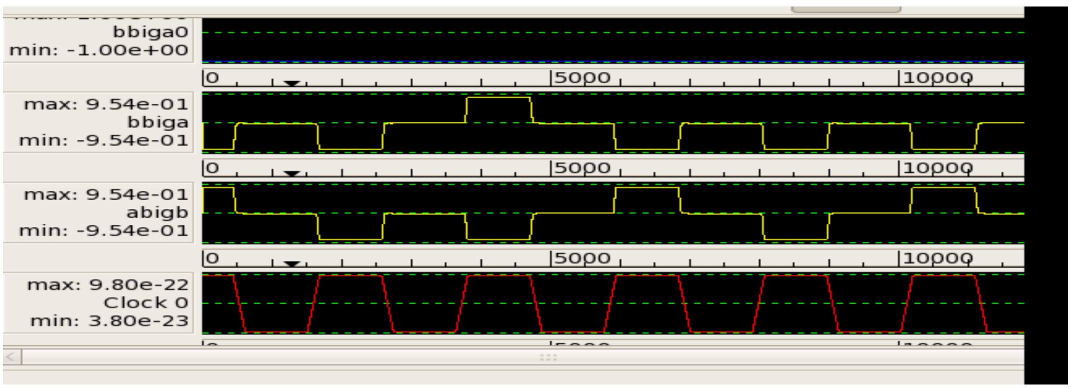


Fig.7. a)T1, b)T2 c)T3 d)T4 e)C1 f)C2

The fundamental QCA logic primitives also include a QCA wire and QCA inverter. This factinitiated a number of studies aimed to find an effective method for synthesis of QCA based logic structures.





A QCA clock consists of four phases which are called Switch, Hold, Release, and Relax.During the Switch phase, the inter-dot barriers are slowly raised and the QCA cells become polarized according to the state of their drivers (that is, their input cells). During the Hold phase, the inter-dot barriers are kept high and the QCA cells retain their states. In the Release phase, the barriers are lowered and the cells are allowed to relax to an unpolarized state. Finally, in the Relax phase, the barriers are kept low and the cells remain unpolarized.

VI. PROPOSED METHOD

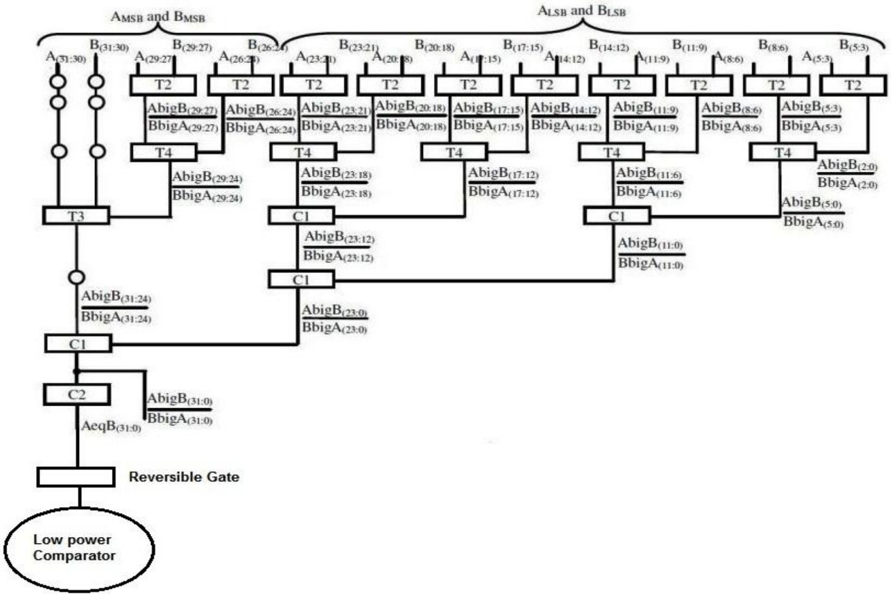


Fig.8. proposed QCA comparator tree.

In proposed system the reversible gates logic are used to reduced the power and also leakage current. The information loss also be reduced.

VII. CONCLUSION

A device paradigm based on QCA cell so offer the opportunity to break a way form FET based logic and to exploit the quantum effects that come with small sizes. In this new paradigm the basic logic cell elements no longer a currents switch, but a small array of quantum dot and the logic tateisen coded as the position of electrons with a quantum dot cell.

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