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A Novel Multilevel Inverter Converter Topology With Reduced Number Of Power Electronic Component

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Abstract— The word "Multi-level inverter" has become more popular, due to its rising demand in the industry because of capability of handling high power high voltage with less THD, reduced switching losses, good power quality. This paper presents a proposed MLI topology to reduce the number of component count even for a large number of voltage levels and it is suitable for symmetrical structure. This proposed topology result in the reduction of power switches, power diode and gate driver circuit due to which further it decreases the installation cost and area as compared to conventional topology. The working demonstration of proposed topology is given with the help of single-phase 9-level inverter. This topology is tested and simulation result is obtained with the help of computer based MATLAB Simulink software.

Keywords— Multilevel inverter (MLI), Pulse width modulation(PWM), THD, Reduced component count.

I. INTRODUCTION

In the recent era, MLI is very important in the area of high power high voltage application [1]-[4], due to which it has drawn a great attention in industry. It was 1st introduced in the 1970s and 1980s [2]-[3]. MLI has many advantages over the two-level inverter in many ways like low switching frequency, hence reduction in switching losses, lower harmonic, lower common mode voltage, reduced dv/dt stress[5]. MLI produced output voltage waveform as like sinusoidal waveform[7]. By increasing the number of levels of MLI the quality of MLI waveform is increased but by increasing the levels, the number of counts of semiconductor devices and gate driver circuit increase. Due to increase in number of devices, the size and complexity of circuit increase. There are several MLI topologies that have been proposed are: 1) Diode-clamped MLI (DCMLI), 2) Flying-capacitor MLI (FCMLI), 3) Cascaded H-bridge MLI (CHBMLI) [8]-[11]. Which are further subdivided into symmetrical and asymmetrical MLI. CHBMLI was 1st introduced the after DCMLI followed by FCMLI [1]. All these conventional topology requires different techniques to produce output voltage levels. The CHBMLI is a connection of H- Bridge with a Separate DC link for each bridge cell so it is easily controllable [13]. The DCMLI series capacitor bank where as in a FCMLI floating capacitor is used in order to clamp the output voltage [18]. Conventional MLI has some disadvantage that by increasing the number of voltage levels, number of switching deices given by 2(N+1) also increased [1]-[3]. Where N is the number of voltage levels. Due to increase in number of voltage levels circuit become complex, efficiency and reliability may be reduced [14]. In this paper a novel MLI topology is proposed in which H-bridge is used with four other power switches to generate 9-level output voltage waveform. This approach significantly less number of power switches needed as compare to conventional topologies. Due to required less number of power witches, cost and complexity decreases [15]-[17]. The main motive of this paper is to reduce the total number of power switches, diode, capacitor and cost of the circuit. A 9-level proposed MLI topology is introduced in this paper using different PWM [20] techniques to generate output voltage levels.

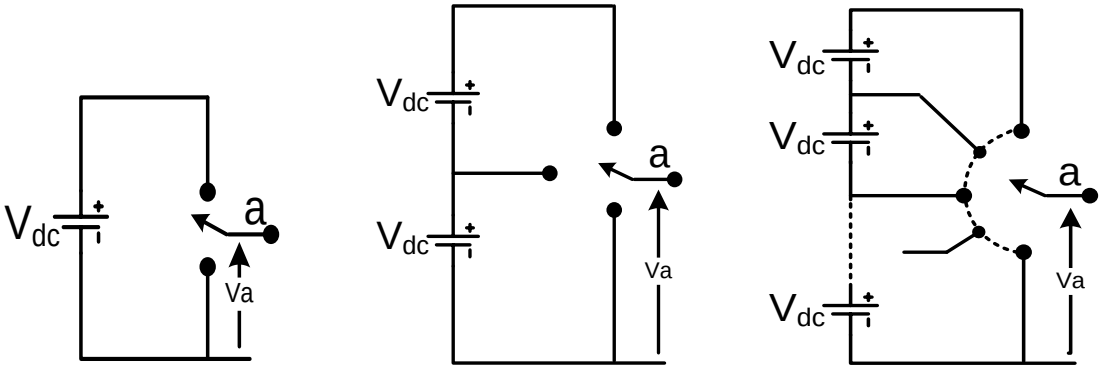

Figure 1. Single leg Multilevel inverter (a) Two level (b) Three level (c) M level.

II. PROPOSED TOPOLOGY

According to the motive of this paper, the structure of the proposed topology is introduced in which it reduces the overall number of switching devices from conventional MLI and its working principle is explained with the help of single-phase 9-level inverter. Output voltage, current waveform is also presented.

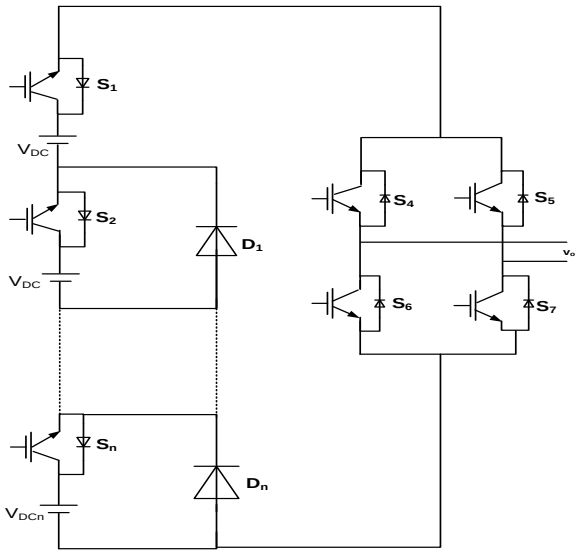

Figure 2. Generalized single-phase structure of proposed topology.

2.1. Generalized structure

The generalized structure of single-phase proposed topology is shown in Fig.2. it consist of n number of DC input source. They have less count of power devices as compare to the conventional MLI. It has one cell of H-bridge with the other power switches as shown in Fig.2. In 9-level MLI, it consists of one cell of H-bridge with four main switches and four auxiliary switches with three diodes. It has four separate DC source such as 9-level cascaded H-bridge MLI. For different number of voltage levels, the proposed topology can be easily extended by increasing the middle part of the circuit. The proposed topology is a symmetrical topology with all DC voltage sources has equal value.

2.2. Working principle

The working principle of the proposed topology is given with the help of single-phase 9-level MLI with four input DC source, as shown in Fig.3. It has eight power switches in which four are connected in series with separate input DC source. The operating modes are shown in Fig.4 and are summarized in Table I. With the help of operating modes as shown in Fig.4, the load is supplied with 9-levels +Vdc, +2Vdc, +3Vdc, +4Vdc, Zero, -Vdc, -2Vdc, -3Vdc, -4Vdc.

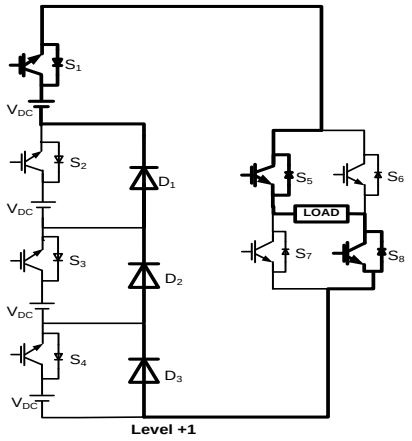

Figure .(a)

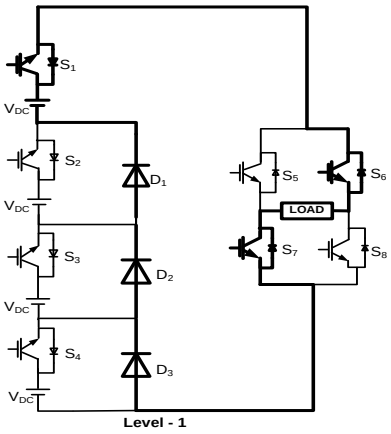

Figure .(b)

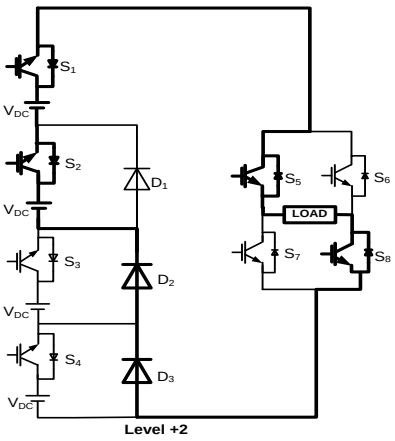

Figure.(c)

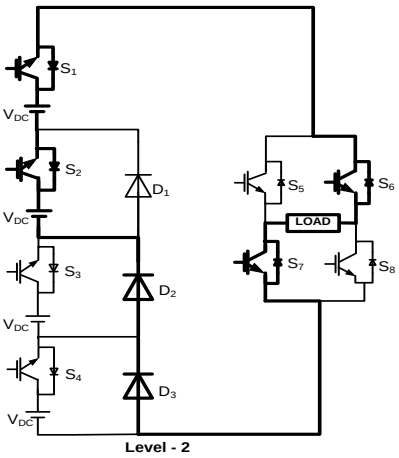

Figure.(d)

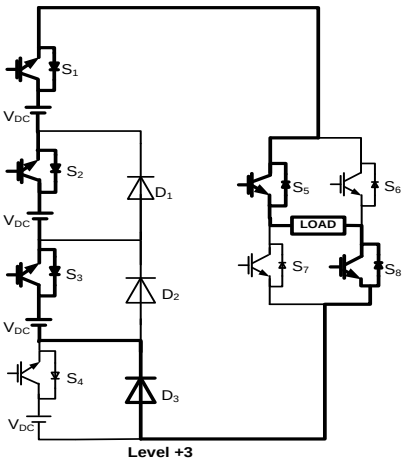

Figure.(e)

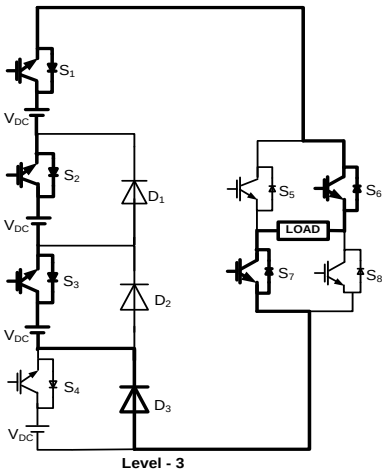

Figure.(f)

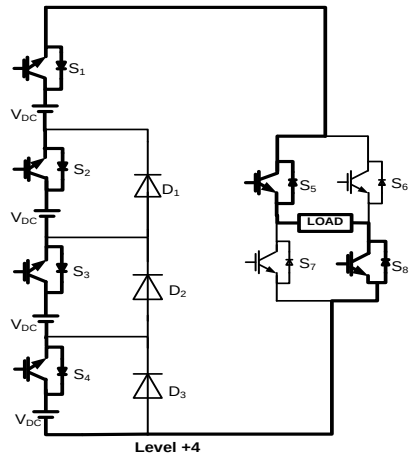

Figure.(g)

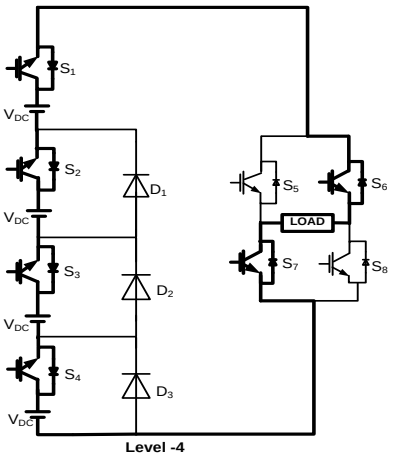

Figure.(h)

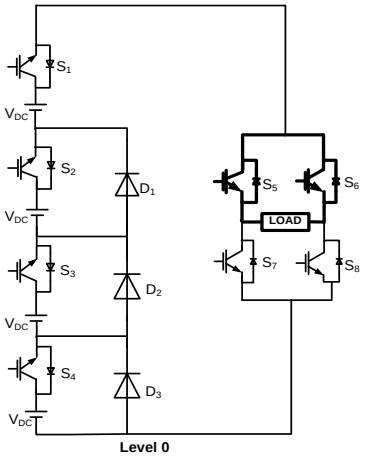

Figure. (i)

Figure.4. Figure (a), Figure (b), Figure (c), Figure (d), Figure (e), Figure (f) , Figure (g), Figure (h) and Figure (i) are switching combination of 9-level MLI.

Table-1

Mode	Switching states (1 = ON; 0 = OFF)								Output Voltage
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	
+4	1	1	1	1	1	0	0	1	+4Vdc
+3	1	1	1	0	1	0	0	1	+3Vdc
+2	1	1	0	0	1	0	0	1	+2Vdc
+1	1	0	0	0	1	0	0	1	+Vdc
0	0	0	0	0	1	0	0	1	0
-1	1	0	0	0	0	1	1	0	-Vdc
-2	1	1	0	0	0	1	1	0	-2Vdc
-3	1	1	1	0	0	1	1	0	-3Vdc
-4	1	1	1	1	0	1	1	0	-4Vdc

III. CONTROL AND MODULATION STRATEGIES

Single-phase 9-levels MLI require 8 triangular carriers wave. There are four different PWM strategies as given below:-

3.1. Phase disposition pulse width modulation (PD PWM):-

In PD PWM the entire (N-1) carrier are in same phase with having same amplitude and frequency. In this proposed topology eight carrier wave s compared with one sinusoidal reference wave. For N voltage levels of MLI N-1 carrier signal is used. Fig.5 shows the PD PWM strategy.

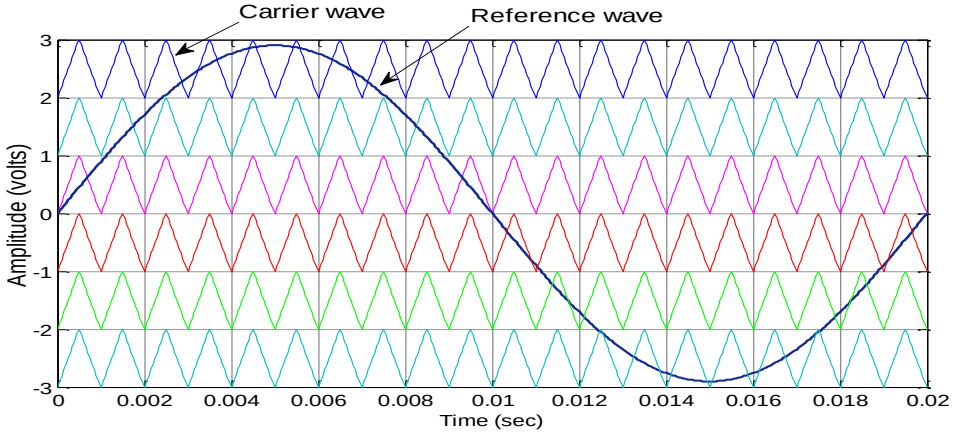

Figure. 5: Carrier arrangement for PDPWM strategy.

3.2. Phase opposition disposition pulse width modulation (POD PWM):-

In POD PWM strategy all (N-1) carriers signal are I same phase to each other above the zero-axis with same amplitude and frequency but carrier wave below zero-axis is 180^0 out of phase to above zero-axis carrier waveform.

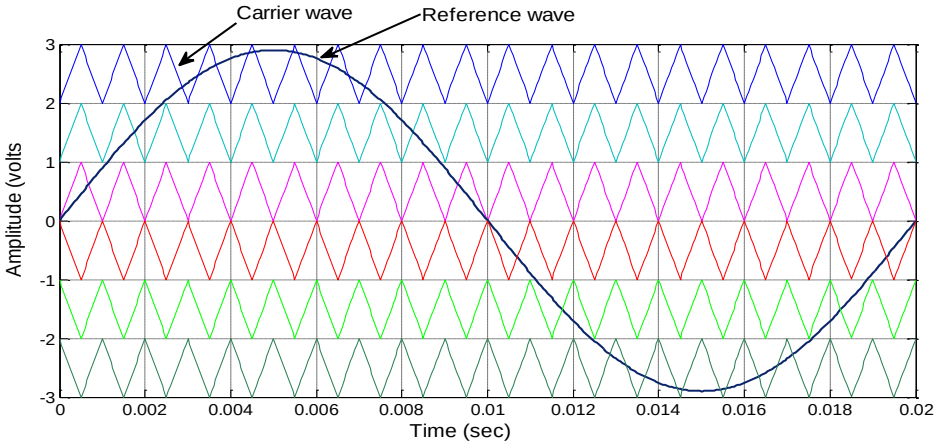

Figure. 6: Carrier arrangement for PODPWM strategy.

3.3. Alternate phase opposition disposition pulse width modulation (APOD PWM):-

In APOD PWM strategy all the carrier wave is out of phase with its neighboring carrier wave by 180^0 but all carriers has same amplitude and frequency.

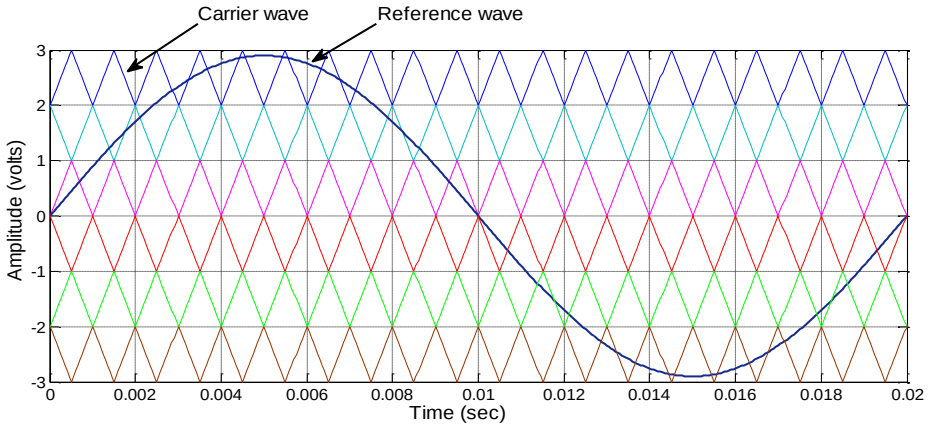

Figure. 6: Carrier arrangement for APODPWM strategy.

3.4. Carrier over-lapping pulse width modulation (CO PWM):-

In CO PWM all the carrier wave with same frequency and peak to peak amplitude overlap each other.

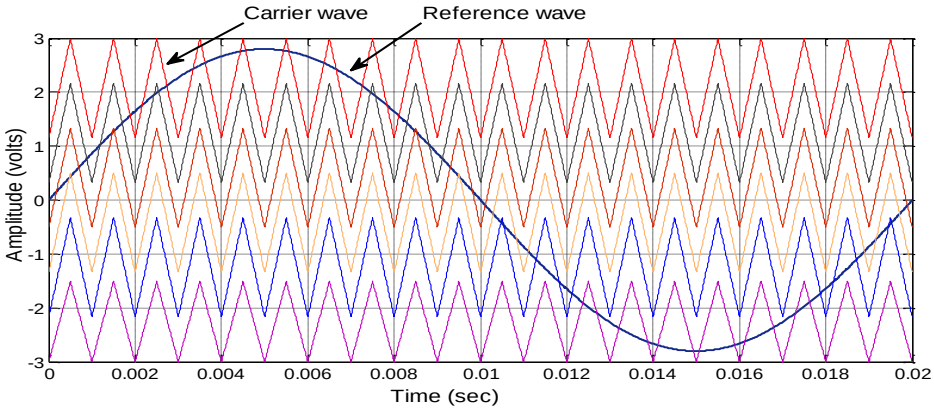

Figure. 7: Carrier arrangement for COPWM strategy

IV. SIMULATION RESULT

With the help of MATLAB Simulink, output voltage and current waveform is obtained as shown in Fig.8 and Fig.9. Table II shows its Comparison between different multilevel inverter topologies. The simulation parameters are as following R= 10 ohm, L= 1mH and DC source V is 400V; carrier signal frequency is 2 kHz and this paper has four PWM techniques are used PD, POD, APOD and CO with different modulating index(Ma). THD of four PWM techniques are shown in Fig.10 to Fig.13. .The harmonic spectrum is carried out by using the FFT analysis in MATLAB/Simulink.

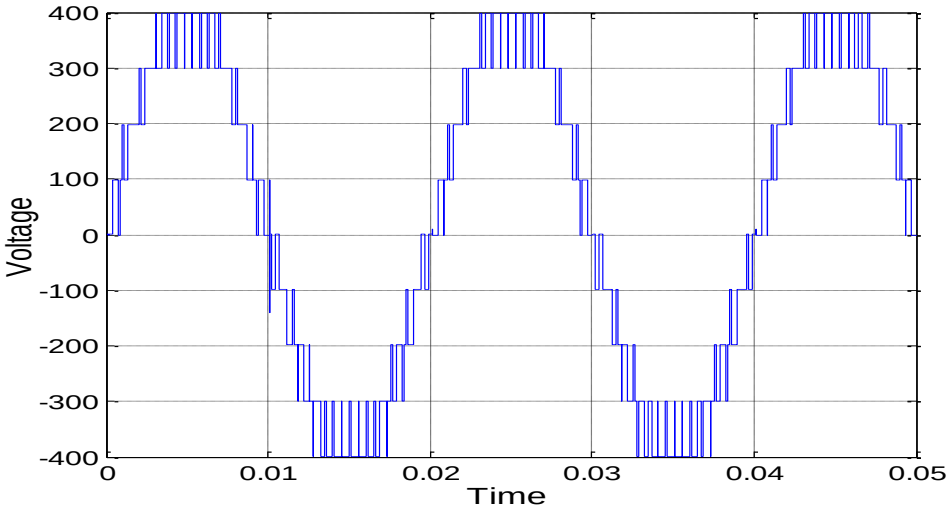

Figure. 8: Output voltage waveform of single-phase 9-level MLI.

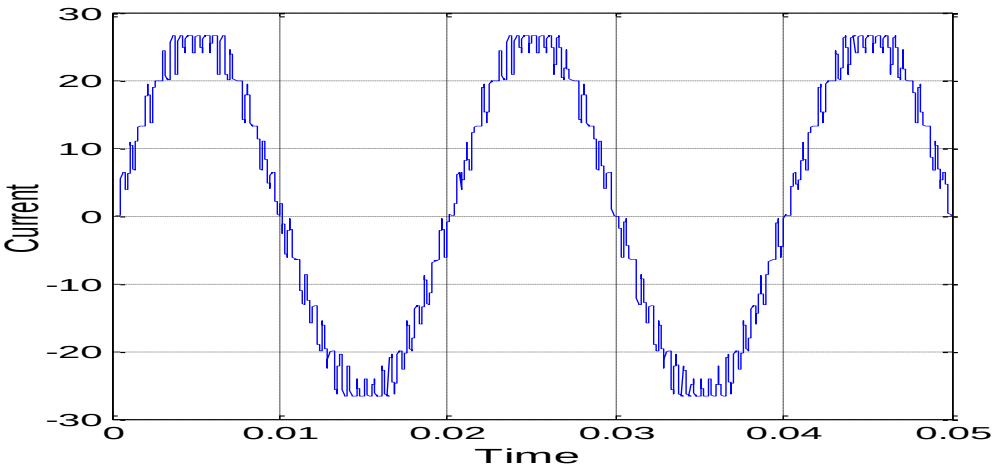

Figure. 9: Output current waveform of single-phase 9-level MLI.

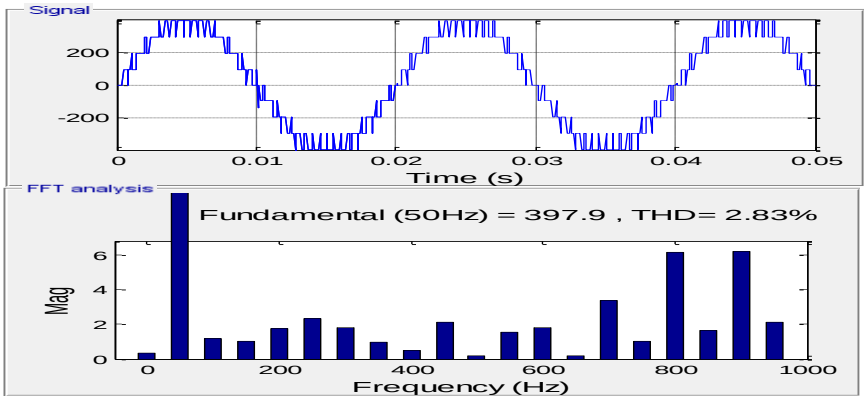

Figure. 10: FFT analysis by PDPWM for R-L load (Ma=0.9, Mf=40)

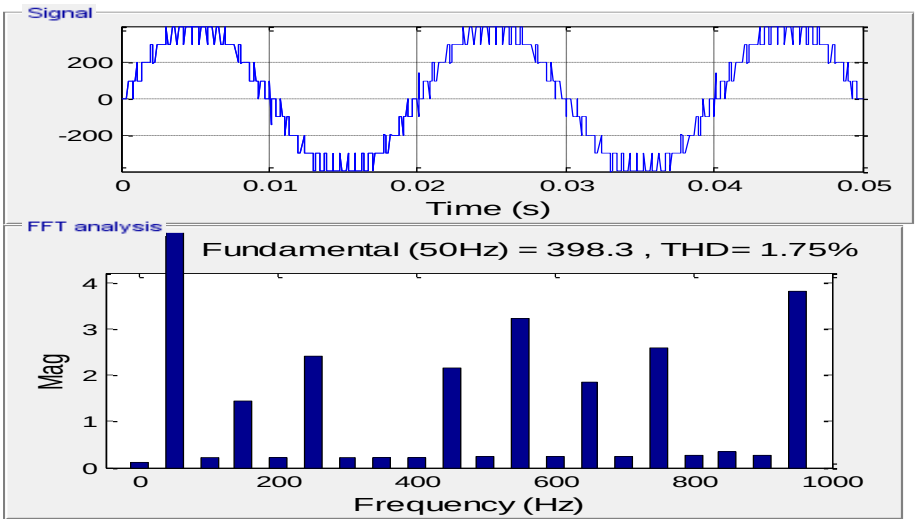

Fig. 11: FFT analysis by PODPWM for R-L load (Ma=0.9, Mf=40).

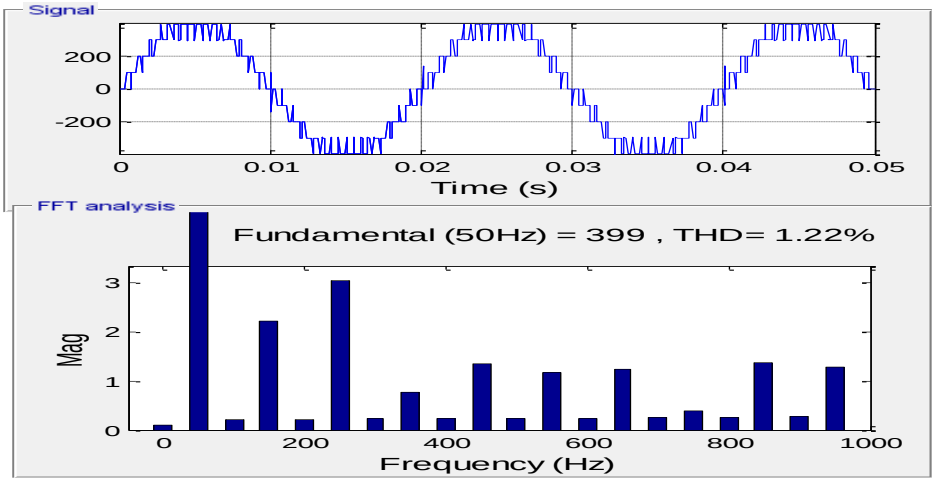

Figure. 12: FFT analysis by APODPWM for R-L load (Ma=0.9, Mf=40).

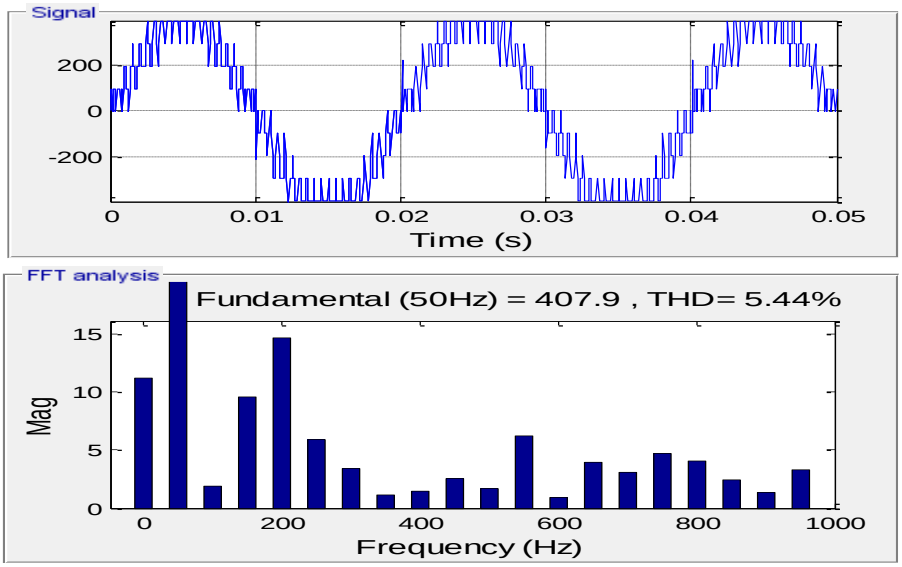

Figure. 13: FFT analysis by COPWM for R-L load (Ma=0.9, Mf=40).

The required number of components for 9- level MLI is shown in Table II. Comparison between different multilevel inverter topologies

Table-II

Inverter topologies	CHB	NPC	Flying capacitor	Proposed topology
Power switches	16	16	16	8
Main diode	0	0	0	3
Clamping diode	0	56	0	0
DC bus Capacitor	0	8	8	0
Flying capacitor	0	0	21	0
DC source	4	1	1	4

Table-III

THD analysis b/w different PWM techniques for 9-level MLI.

PWM Technique	Modulation Index			
	1	0.9	0.8	0.7
PD PWM %THD	2.83 %	2.97 %	3.1 %	3.13 %
POD PWM % THD	1.17 %	1.32 %	1.53 %	1.82 %
APOD PWM % THD	1.22 %	1.36 %	1.39 %	1.53 %
CO PWM % THD	5.44 %	5.57 %	6.10 %	6.27%

IV. CONCLUSION

In this paper, a 9-level multi-level inverter using this topology is proposed with different PWM techniques and proposed MLI topology with different PWM techniques is used to generate 9-level output phase voltage. With the help this topology 9-level MLI output voltage with less count of power switches as compare to other conventional MLI topologies. Simulation results show the performance of single-phase 9-level MLI with different PWM techniques. Harmonic analysis is done with the help of MATLAB software.

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