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Design of Pulse Triggered Flip Flop Using Conditional Pulse Enhancement Technique

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Abstract- In this paper a low power and low area pulse triggered flip flop has been analyzed. The dominant part of this VLSI process design is power consumed by the clock. The flip flop is the basic element of memory element and clocked signal. The conventional TSPCFF is use to one extra NMOS transistor to shorten the delay and power. The conventional design removes the long discharging problem and reduces D to Q delay. Thus, the proposed design reduces the number of NMOS transistors stacked in the discharging path. The proposed design is compared with the some conventional design EP-DCO, CDFF, TSPCFF. The schematic and post-layout simulations have been done using tanner tool at 250nm VLSI technology. The proposed design has resulted in reduction of overall power consumption in comparison to some conventional technique EP-DCO, CDFF, TSPCFF respectively. The results also show some reduction in leakage power. The average power consumption of proposed pulse triggered flip flop using pass transistor logic is 16uw and the number of transistors used 18.

Index Terms: low power, pass transistor, pulse, flip- flop, pulse triggered.

I.INTRODUCTION

Flip-flops (FFS) are the fundamental storage parts used extensively altogether sorts of digital styles. In particular, digital styles today typically adopt intensive pipelining techniques and use several FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power [1]. Pulse triggered FF (P-FF) has been thought of a preferred various to the traditional master-slave based FF with in the applications of high speed operations [2]-[5].

Flip-flop can be simple (transparent or opaque) or clocked (synchronous or edge-triggered). Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits. The simple ones are commonly called latches using this terminology, a latch is level-sensitive, whereas a flip-flop is edge-sensitive. When a latch is enabled it becomes transparent, a flip-flop's output only changes on a single type (positive or negative going) of clock edge.

If the power consumed by the flip-flop is reduced then there will be reduction on total power consumption of the clock system. Pulse triggered flip-flop (PT-FF) is considered as an alternative for the conventional transmission gate (TG) based or master-slave based edge triggered flip-flops. A PFF consists of single latch as compared with two latches in the conventional transmission gate (TG). This gives better power performance and speed. A PFF consists of a latch and pulse generator. If the width of the triggered pulse is narrow then the latch acts like an edge triggered flip-flop, these are of two types: implicit type and explicit type. In an implicit type, the clock generation is built in logic with latch. In an explicit type, the lock generation and latch are separate.

In this brief, are present a novel low –power P-FF design based on a conditional pulse enhancement scheme. The pass transistor logic functions using output of an nmos pass network is restored to

achieve the maximum voltage swing at the output node, as low rise and fall times. Achieve low area, high speed of operation, and low power dissipation. Traditional pass transistor logic designs with respect to the transition delays the area and the power dissipation. This Method implemented by introducing a simple pass transistor for extra signal driving

II. EXISTING SYSTEM

2.1 Design Approach

The power of the FF is mostly dissipated in the operation of clock-related NMOS transistors, and reduced the number of transistor and to reduce load capacitance in internal nodes, also reduced discharging path.

2.1.1 True Single - Phase Clocking Flip-Flop

Flip-flop used for the high speed digital design,short latency, is to have a simple and signal feed through scheme. A family of static and dynamic latches with such characteristics is true single-phase clocking(TSPC) [4]. TSPC latches can be combined in several different ways to implement edge triggered flip flop.

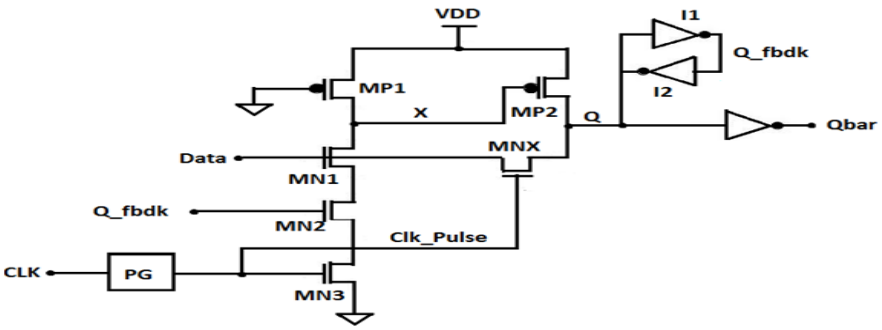

Fig.1. Pulse triggered flip-flop(P-FF)

If the pulse generated externally, using a pulse generator, the circuit suffer from the charge sharing. So avoiding charge sharing, this local pulse generation allows better control of the pulse width, so that a very narrow effective pulse can be produced, an reduce potential race-through problems and also improve the noise sensitivity of the circuit.

a) Pulse Triggered Flip-Flop Design

The PFF design adopts a signal feed-through scheme to improve this delay. The design also employs a static latch structure and a conditional discharge scheme to avoided switching at an internal node. This system solving long discharging path problem in conventional explicit type pulse- triggered flip-flop. When a clock pulse arrives and there is no data transition occurs. The input data and node Q at the same level.

III. CIRCUIT REALIZATION

In Fig. 3. shows the proposed pulse triggered flip-flop design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1.

The proposed design, as shown in Fig. 3, adopts two measures to overcome the problems associated with existing PFF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." this PFF design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at nodeZ can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." It steps in when node X is discharged VTP below the VDD. This provides additional boost to node Z (from VDD-VTH to VDD).

The Principle of operation pulse triggered FF design is explained as follows

- When the clock signal is "low", input signal Data is "0", output signal Q is "0 and control signal Q_fdbk is "1".
- When the clock signal is "low", input signal Data is "0 - 1",as the control signal Q_fdbk is "1" at the previous state.
- when the clock signal is "Low-High" , input signal Data is "0-1", as a normal state transformation occurs, the second N-transistor N2 and the third transistor N3 are set ON for an inverter delay period, and each sends a VDD -Vtn signal to the node of transistor N1.
- When the clock signal is "High-Low", input signal Data is "1-0", the clock generator is OFF, output signal Q maintains the captured value of the previous state.
- When the clock signal clock signal is "Low-High", data is "1-0", the clock generator OFF; output signal Q maintains the captured value of the previous state.

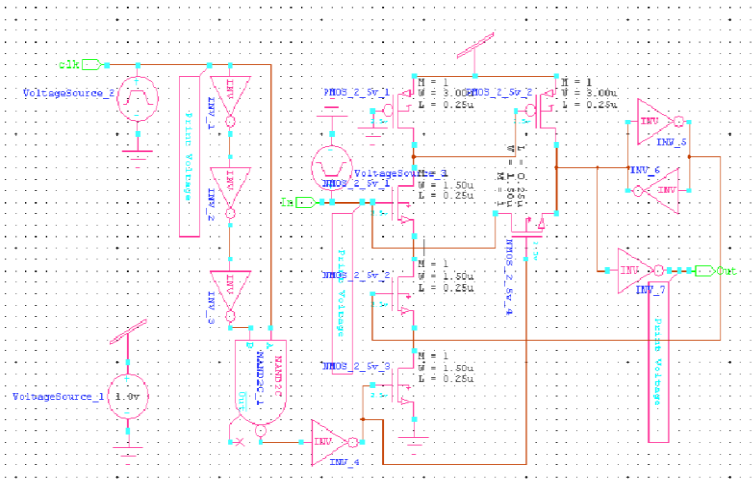

Fig.2. Schematic diagram of existing P FF

IV. PROPOSED SYSTEM

The proposed pulse triggered flip flop design shown in fig 4. it employs a static latch structure and at two- input pass transistor logic (PTL)- based AND gate is implemented with NMOS pass transistor in existing pulse triggered with signal feed through scheme. By using the pass transistor logic family we are designing this circuit as well as by using the pass transistor logic we are using only one locking transistor so it will be consume less power in the clocking network of the flip flop when compared to all other circuit. As well as proposed pulse triggered flip flop having only 18 transistors.

In proposed flip flop the clocking transistor is used to control the charge of transistor N5. Since the two inputs of AND logic to control the discharge of transistor N1 are mostly complementary, the output node Z (in between N2 and N3) is kept at zero most of the time. When both input signals equal to "0"(falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N3 and N4 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N5 by a time span defined b the delay inverter inv3. The switching power at node Z can be reducing due to a diminished voltage swing.

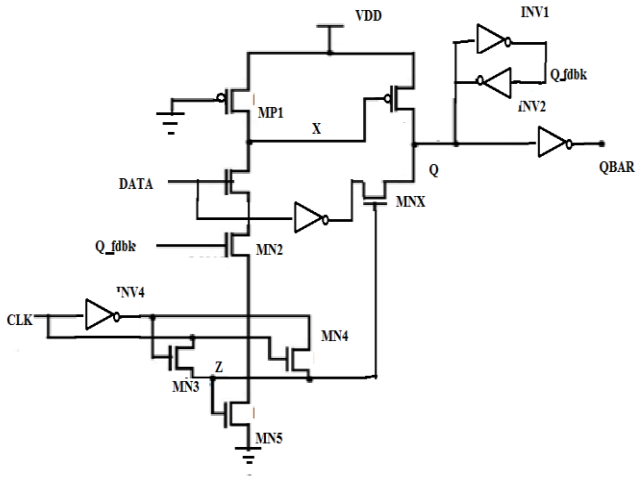

Fig.3. proposed PTL

The switching power at node Z can be reduced due to a diminished voltage swing. When a clock pulse arrives, if no data transition occurs, i.e., the node Q and the input data are at the same level, on current passes through pass transistor N6, which keeps the input stage of the flip flop from any driving effort. If a "0" to " 1" data transition occurs, node X is discharging to turn on transistor P2, which then pulse node Q high. Since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

In the proposed pulse triggered flip flop design the area and average power consumption can be reduced when compared to existing data close to output flip flop design. It will be having much reduced power and area when compared to the designs. At the same time due to the reduced number of transistor count we can reduce the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to flip flop design.

The proposed model is an implicit type pulse triggered flip-flop with a conditional pulse enhancement scheme. There are two measures employed to overcome the draw backs in the conventional designs. Due to the presence of the large number of transistors in the discharge path the delay is high and also large power is consumed in power-up of the transistors. So, the number of nMOS transistors in the discharging path should be reduced. Also there is a need to increase the pull down strength when the input data=1. So there is a need to conditionally enhance the pull down

strength when input data is "1." This design inherits the upper part of the SCCER design.. Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero most of the time. There is a floating node when both input signals equal to "0". When there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node.

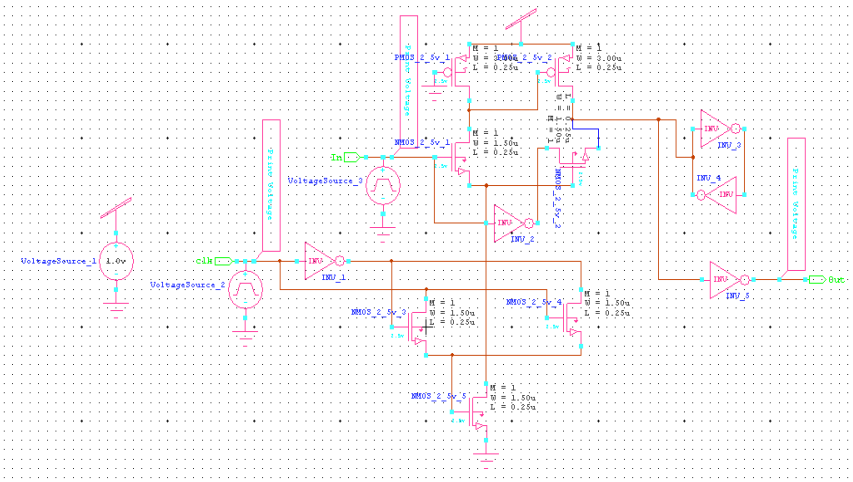

Fig.4. Proposed Schematic Diagram

V. SIMULATION RESULT

The proposed PFF was designed and implemented in a Generic 250 nmCMOS process.

The proposed design adopts a conditional pulse enhancement technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid switching at an internal node. However, there are three major differences that TSPC latch structure and make the proposed design distinct from the previous one.

In Fig.3. shows the proposed pulse triggered flip-flop design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1.

The proposed design, as shown in Fig. 3, adopts two measures to overcome the problems associated with existing PFF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." this PFF design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at nodeZ can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked

transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." It steps in when node X is discharged VTP below the VDD. This provides additional boost to node Z (from VDD-VTH to VDD).

Proposed Method

The simulation Output of pulse triggered flip-flop is shown below

```
File   Edit   Format   View   Help
 1.006714e-009   1.0067e+000   1.0067e+000  -2.5329e-003
 1.141321e-009   1.1413e+000   1.1413e+000  -6.2457e-003
 1.328301e-009   1.3283e+000   1.3283e+000  -7.2108e-003
 1.588198e-009   1.5882e+000   1.5882e+000  -1.1911e-002
 1.911275e-009   1.9113e+000   1.9113e+000   3.8440e-001
 2.219730e-009   2.2197e+000   2.2197e+000   9.5340e-001
 2.373957e-009   2.3740e+000   2.3740e+000   1.0106e+000
 2.588268e-009   2.5883e+000   2.5883e+000   9.9313e-001
 2.962793e-009   2.9628e+000   2.9628e+000   1.0053e+000
 3.492509e-009   3.4925e+000   3.4925e+000   9.9556e-001
 4.176490e-009   4.1765e+000   4.1765e+000   1.0038e+000
 5.000000e-009   5.0000e+000   5.0000e+000   9.9657e-001
 5.249999e-009   5.0000e+000   5.0000e+000   9.9956e-001
 7.250000e-009   5.0000e+000   5.0000e+000   9.9999e-001
 9.250000e-009   5.0000e+000   5.0000e+000   1.0000e+000
 1.000000e-008   5.0000e+000   5.0000e+000   9.9999e-001

*  BEGIN NON-GRAPHICAL DATA

Power Results
VVoltageSource_3 from time 1e-009 to 1e-008
Average power consumed -> 2.868905e-003 watts
Max power 4.235946e-003 at time 5e-009
Min power 2.379554e-005 at time 1.3283e-009

VVoltageSource_2 from time 1e-009 to 1e-008
Average power consumed -> 3.303244e-005 watts
Max power 1.179825e-004 at time 5e-009
Min power 5.171202e-010 at time 1e-008

VVoltageSource_1 from time 1e-009 to 1e-008
Average power consumed -> 5.791615e-004 watts
Max power 8.340150e-004 at time 5e-009
Min power 2.739474e-005 at time 2.21973e-009

*  END NON-GRAPHICAL DATA
*
*  Parsing                          0.04 seconds
*  Setup                            0.02 seconds
*  DC operating point               0.00 seconds
*  Transient Analysis               0.02 seconds
*  Overhead                         2.61 seconds
*  ---------------------------------------------
*  Total                            2.69 seconds

*  Simulation completed

*  End of T-Spice output file
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Fig.5. Schematic output of power calculation

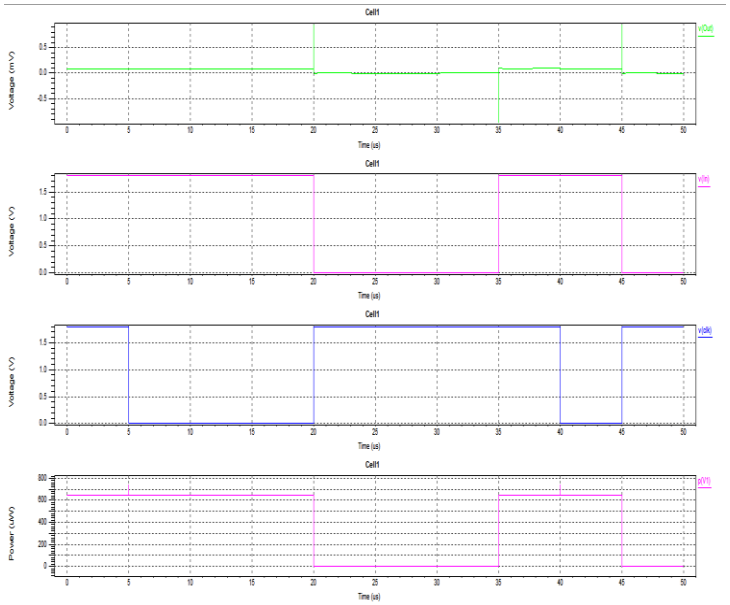

Fig.6. PLT power waveform in tanner tool

VI. COMPARISION

The comparison between the existing and proposed design is sown in Table 1.

FF DESIGNS	No of transistors	Layout width
CD FF	30	28
SCD FF	31	26
EP-DCO FF	28	23
P FF	24	19
PTL	18	15

Table 1 No of transistor using various flip flops

VII. CONCLUSION

In this paper, the proposed pulse triggered flip flop is designed with two-input pass transistor logic (PTL) based AND gate is implemented in existing pulse triggered flip flop with signal feed through scheme of pseudo n-MOS logic pass transistor. This design is combination of conditional pulse enhancement scheme and existing pulse triggered flip flop with signal feed through scheme. The average power consumption and number of transistor count should be reduced by proposed pulse triggered flip flop design. It will be reduced power, at the same time reduced number of transistor count and also reduced the delay. Thus we are reducing the overall switching delay and power.

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