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REDUCING POWER CONSUMPTION USING CLOCK GATING TECHNIQUE IN FLIPFLOP

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Abstract— In this paper describes about reducing the power consumption of a synchronous digital system by minimizing the total power consumed by using the clock signals. To reducing the clock signals, gating techniques can be used. The synchronous design operates at highest frequency that derives a large load because it has to reach many sequential elements throughout the chip. Thus clock signals have been a great source of power dissipation because of high frequency and load. Clock signals do not perform any computation and mainly used for synchronization. Hence these signals are not carrying any information. So, by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. A new counter using clock gated flip-flop is presented in this paper. The circuit is based on a new clock gating flip flop approach to reduce the signal's switching power consumption. It has reduced the number of transistors. The proposed flip-flop is used to design the counter circuit.

Keywords— Clock gating, clock networks, Dynamic power consumption, Flip-Flop, Latch.

I. INTRODUCTION

Reducing the power consumption in Very Large Scale Integrated circuit has very important. It is used to improve the battery life. The power consumption in a digital circuit is two types. 1) Static power and 2) Dynamic power. [1]

In static power dissipation occurs when there is no change in input of the circuit. The static power is power consumed, while there is no circuit activity. For example the power consumed by D flips flop, when either the clock signal (or) the D input have active input.

In Dynamic power dissipation occurs when the input signal has switching active state. The dynamic power dissipation is caused during the capacitance have charging and discharging process. The input signal can be change in unnecessary, the logic transition occurs at the output. The dynamic power dissipated occurs when the output does not change in the logic state.

Dynamic power dissipation in a circuit is given as

$$P_D = \alpha\, C_L V_{DD}^2\, F$$

α –Switching activity, F- Operating frequency, C_L- Load capacitance, V_{DD} – Supply voltage.

To reducing the dynamic power consumption the clock gating techniques can be used. This technique is used in many synchronous circuits for reducing the dynamic power dissipation. It is also used to reduce the clock power [2]. The clock gating techniques is used to saves more power by adding more logic to the circuit. In a sequential circuit consists of more number of blocks. All the blocks are not working in at the same time. So the dynamic power consumption is reduced. In the Flip flop, the switching states consume more power. But circuit is not being switched, so power consumption is zero and at the same time, only the leakage current is incurred. This clock gating technique can also used to save power and area. The clock gating logic is formation of "Integrated Clock Gating" cells. The clock gating logic is removes the more number of Multiplexers.

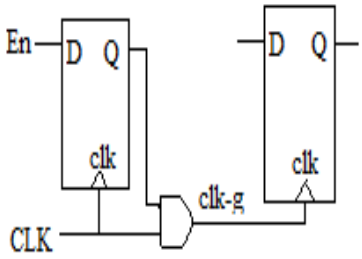

Fig.1. Latch based clock gating.

The latch based clock techniques consists of level sensitive latch and AND gate. The several methods can make use of this technique is the major advantage of this method. The various heuristics to increase the clock gating. The method is called synthesis based. It is most widely used method by EDA tools. The Data- to-clock toggling ratio is used to measure the clock pulse utilization, after the use of this method is very low. The second method is called Data-driven clock gating. The Flip flop can use more number of clock pulse. The clock pulses are gated. So Flip flop cannot change its state in the next clock cycle. A flip flop finds the clock signal is disabled in next cycle by using XOR operation, its output also consider the present input data.

It will be presents in next cycle. The output of XOR gates performs XOR operation to produce the gating signal. The latch and AND gate is used for commercial tools and it is also called "Integrated Clock Gate" [3]. It is used to increasing the power reduction. Data driven gating technique affects from very short time window when the gating circuitry can properly work. The design methodology is very difficult in data driven method. To increasing the power saving, the flip flop can be grouped such that their toggling is highly correlated. [4]-[5].

II. AUTO GATED FLIP FLOP

The Auto Gated Flip Flop circuit is given in Fig.2. [6]

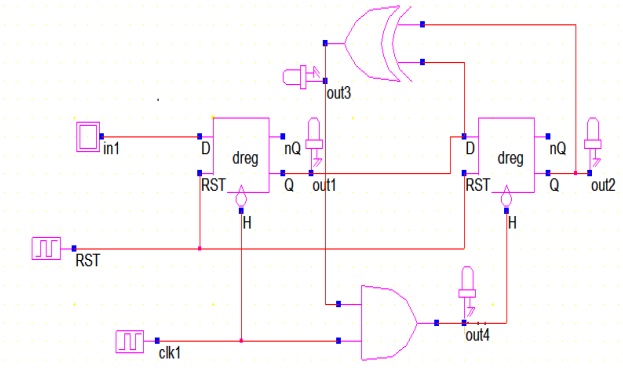

Fig . 2. Circuit for Auto Gated Flip Flop.

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The Flip flop master latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed. [6].

AGFF can also be used for general logic, but with two major drawbacks. First, only the slave latches are gated, leaving half of the clock load not gated. Second, serious timing constraints are imposed on those flip flops residing on critical paths, which avoid their gating.

III. AGFF WITH XOR OUTPUT USED FOR LACG

The clock gating technique has been used to develop to reduce unnecessary power consumptions, like the power wasted by timing components during the time when the system is idle. Especially for flip-flops, clock gating technique means disabling the clock signal when the input data does not alter the stored data. It can be applied from the system level where the entire functional unit can be selectively set into sleep mode, or from the sequential/combinational circuit level where some parts of the circuit are in sleep mode while the rest of the block are operating. But Clock gating does not come for easily. Where the extra logic and interconnects are required to generate the clock enabling signals, and the resulting area and power overhead must be considered. In the case of each clock input of a flip-flop can be disabled, it's yielding maximum clock separation. The clock disabling circuit is shared by a group of several flip-flops in an attempt to reduce the overhead [7].

(i) The implementation of clock gating:

When there is no activity at a register "data" input, there is no need to clock the register and hence the "clock" can be gated to switch it off. If the clock feeds a bank of registers, an "enable" signal can be used to gate the clock, which is called the "clock gating enable". [7].

Hence dynamic power reduces.

There are four different types of optimizing techniques available for clock gating as given below:

1) Latch-free based design.
2) Latch-based design.
3) Flip-flop based design.
4) Intelligent clock gating optimizing option available in Synthesis tool.

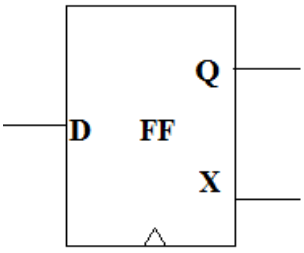

Fig . 3. Symbol of enhanced AGFF with OR output.

Such that the gating technique has been proposed in this paper and it also involves another XOR and OR gates in the circuit, it is used for high clock switching probability.

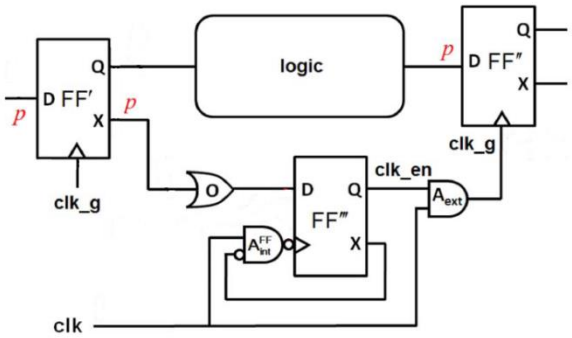

Fig . 4. LACG of general logic.

This consumes a considerable power and area, and the gating logic should therefore be minimized. There are many cases where few target Flip flops depend on similar source Flip flops.

In such cases there is no point in generating separate clock gating signals. The impact of the power savings achieved by Look Ahead Clock Gating on the total power dissipation, that there is also the dynamic power of the logic and the static (leakage) power that is independent of the switching activity.

IV.PROPOSED METHOD

The clock gating technique is described in this paper. It is very useful for reducing the power consumed by digital systems. The synchronous design operates at highest frequency that derives a large load because it has to reach many sequential elements throughout the chip. So by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. A new counter using clock gated flip-flop is presented in this paper.

A counter is a circuit that produces a set of unique output combinations corresponding to the number of applied input pulses. The number of unique outputs of a counter is known as its mod number or modulus. High-frequency operations require that all the FFs of a synchronous counter be triggered at the same time to prevent errors. We use a Synchronous counter for this type of operation.

The synchronous counter is similar to a ripple counter with two exceptions: The clock pulses are applied to each FF, and additional gates are added to ensure that the FFs toggle in the proper sequence.

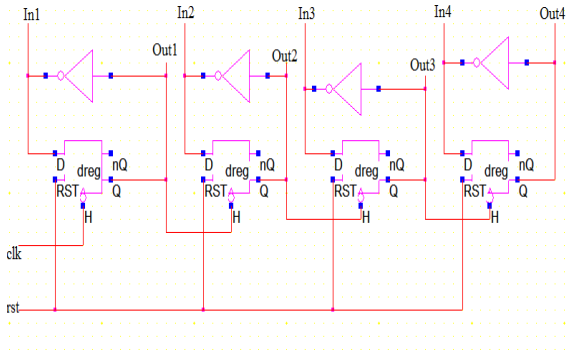

Fig .5. Counter circuit without clock gating.

3 bit synchronous counter having a common clock to all the flip flop Generally counter bits are evaluated at every clock cycle and captured by associated flip flops at every triggering edge of the clock.

V. COUNTER USING CLOCK GATING

In this synchronous counter both conventional D flip flop and data transition look ahead D flip flop were used to generate the binary sequence from “000” to “111” because it will count up to seven bit for every clock signal. But the clock signal flows continuously in the D flip flop independent of the data transition, the increase in the load capacitance results in increase in the power consumption relatively more in D flip flop compare to the data transition look ahead D flip flop. And this Data transition look ahead D flip flop used to minimize the overall power consumption of counters by attempting to eliminate redundant transition in flip flops. The design procedure for synchronous counters is same as that Sequential circuits. Synchronous counter have a regular pattern and can be constructed with complementing flip flops and gates.

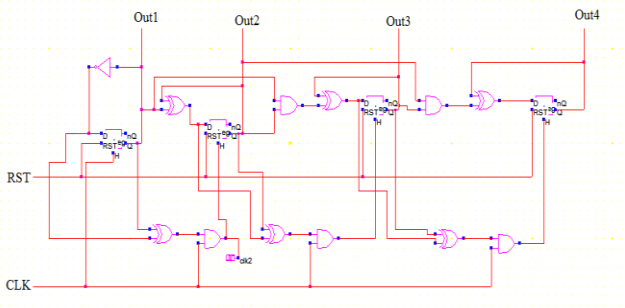

Fig. 6. Counter using clock gated circuit

The new design is based on comparing the flip-flop input and output using a XOR gate which generates a comparison signal. The relation among the clock signal (clk), the comparison signal (cmp), and the generated gated clock signal (clkg) for a positive flip-flop. If clk is 0, and cmp is 0, then the gated clock (clkg) holds its state. When clk is 0 and cmp is 1, then clkg is pulled down. When clk is one, then clkg is pulled high.

Low power designs would prefer the pass transistor approach. In order to overcome the limitation of latches when trying to build registers, edge triggered latches are used, wherein the information flows from the input D to the output Q only at a rising or falling edge of the clock. The latch is commonly known as D- Flip Flop or D-register.

VI. RESULT AND DISCUSSION

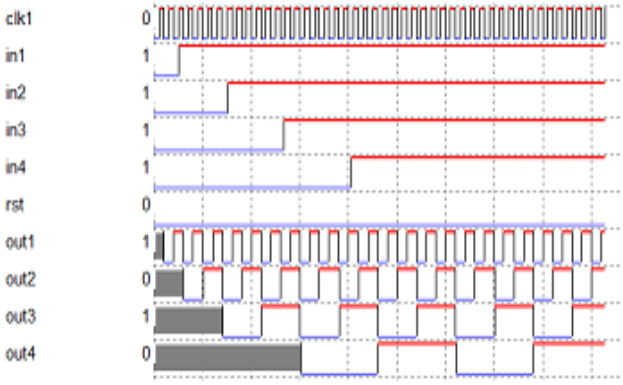

Fig .7. Output waveform for counter circuit

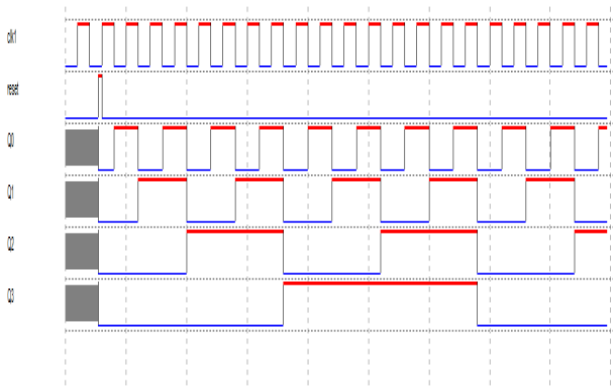

Fig .8. Output waveform for Counter circuit using clock gating

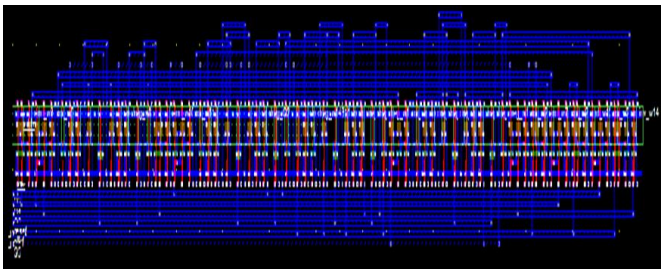

Fig .9. Layout for counter circuit using clock gating.

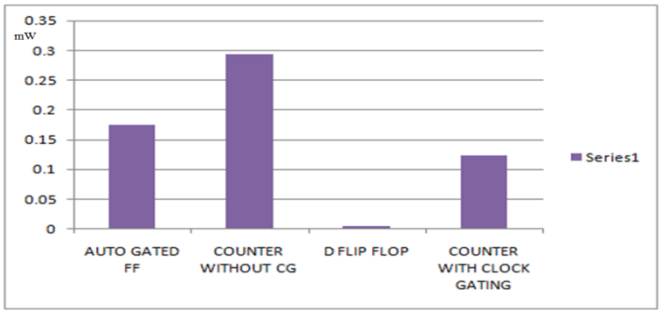

Fig .10. Graphically representation of power consumption

VII. CONCLUSION

A new counter using clock gated flip-flop is presented in this paper. The circuit is based on a new clock gating flip flop approach to reduce the signal's switching power consumption. It has reduced the number of transistors. A new counter using clock gated flip-flop is presented in this paper. The circuit is based on a new clock gating flip flop approach to reduce the signal's switching power consumption. It has reduced the number of transistors.

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