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A voltage-mode circuit structure using FinFet Transconductance Topology

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Abstract— FinFet is evolved to overcome Moore's law limitations in nanometer regime. Transconductance circuit produces differential output currents, when differential input voltages are applied. A simple FinFet transconductance circuit structure modified from traditional MOSFET is proposed to preserve both area and power. The proposed design contributes a transconductance gain of 5.247 mA/v for 10 mv peak-to-peak input voltage. Voltage-mode circuit structure of low-power high frequency filters using FinFet transconductance and transimpedance blocks are investigated in this paper. The simulated third-order harmonic distortion with applying a 300 mv (peak-to-peak) differential inputs, remains below -63 dB at 300 MHz frequency.

Keywords— Voltage-Mode Circuits, FinFet, Transconductance Topology, CMOS Filters

I. INTRODUCTION

Finfet devices have been evolving from the silicon-on insulator in order to satisfy increasing need for higher current drive and better channel behavior. It is developed to overcome the physical limits of conventional MOS structures which are becoming more pronounced due to strong short-channel effects and quantum effect, causing the increase in performance to be limited. It is therefore, necessary to look for new device structures to sustain the growth of the VLSI industry in the nanoscale generations. Double-gate silicon-on-insulator (SOI) transistors can be a good technology choice for nanoscale circuits [1]. A three dimension FinFet structure is shown in Figure 1.

The major characteristic of FinFet devices is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate. The thickness of the fin determines the effective channel length of the device. The finFet structure shown in Figure 1 consists of a vertical silicon fin controlled by self-aligned double gate. The characteristics of MOSFET device are the core to investigate the features of finFet devices.

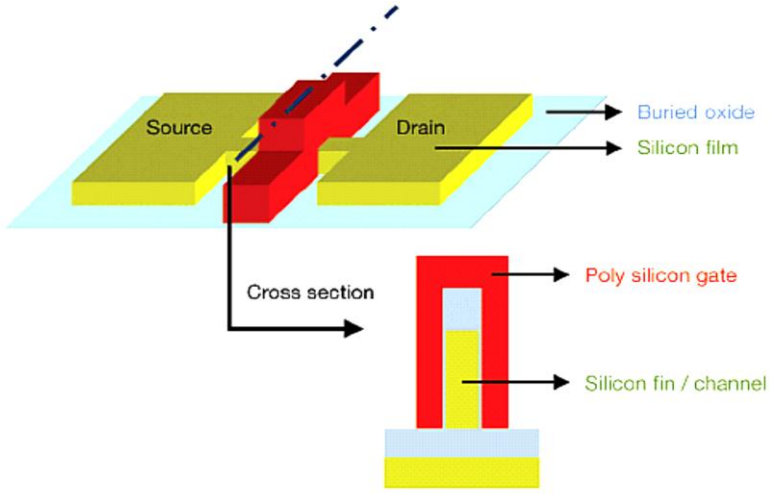

Figure 1. Three dimension FinFet structure

II. ANALYSIS OF FINFET DEVICE

The output characteristics of FinFet n-channel device when $v_g > v_t$ is approximately described by:

$$I_{ds} = 2\mu C_{ox} \frac{W}{L}\left[v_g - v_t - \frac{v_{ds}}{2}\right] v_{ds} \quad (1)$$

When I_{ds} not affected by increasing v_{ds} (saturation condition):

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(v_g - v_t)^2}{2Q} \quad (2)$$

Where, $Q=1+(3t_{ox}/X_d)$, x_d is the depletion layer thickness and t_{ox} is the oxide thickness.
When $v_g < v_t$ (cut-off condition):

$$I_{ds} = \mu \frac{W}{L} kTn_i t_{si} e^{\frac{q(v_g - \Delta\emptyset)}{kT}} \left(1 - e^{-\frac{qv_{ds}}{KT}}\right) \quad (3)$$

Where, $\Delta\emptyset$ is the work function difference between the gate electrode and intrinsic silicon body.

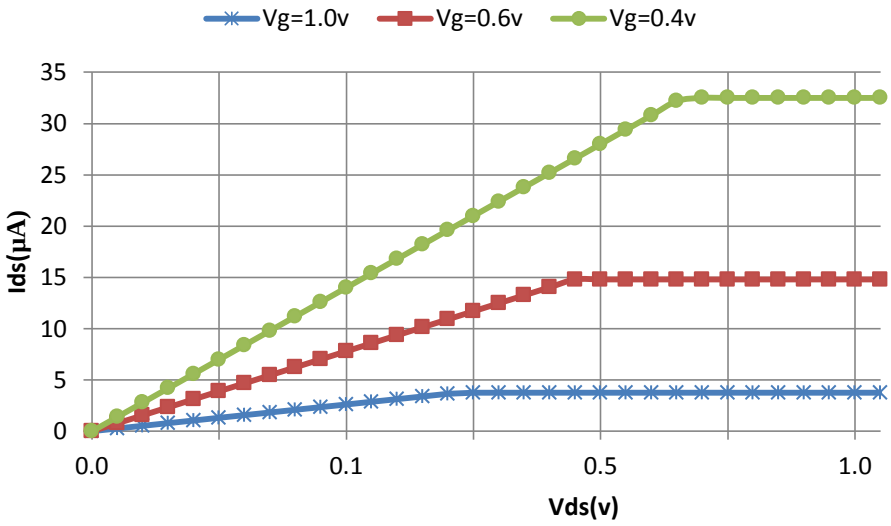

Figure 2.The output characteristics of FinFet (Lch=10µm, tsi=30nm)

Figure 2 Shows the output characteristics of FinFet Device for 10 µm channel length, w_{fin}=150 nm, and t_{si}=30nm.There is no effect of drain voltage over drain current after pinch off voltage.
The ideal characteristics depicted from Figure 3 stated that there is no current flowing upto threshold voltage but after that voltage, the current start increasing.

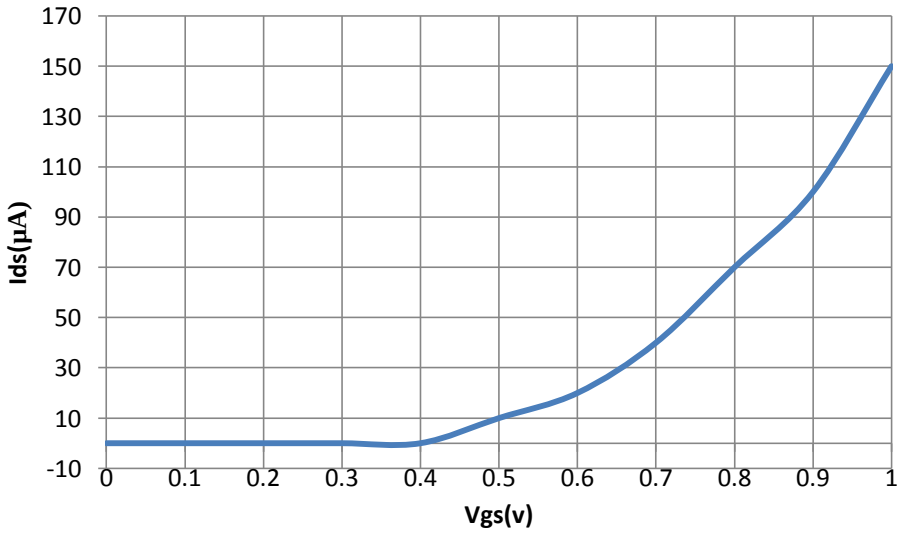

Figure 3 Transfer characteristics of FinFet (Lch=10µm, tsi=30nm)

The sub-threshold current of FinFet where drain current flowing through threshold voltage as shown in Figure 4.

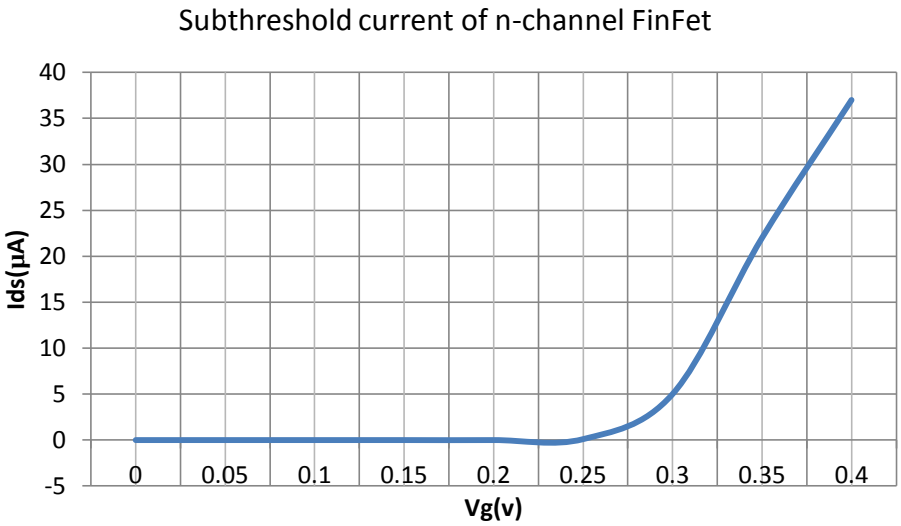

Figure 4 Sub-threshold current of n-channel FinFet (Lch=10 µm Wfin=150nm, tsi=30nm)

III. FINFET INVERTER TRANSIENT RESPONSE

This section investigates the transient response for FinFet technology compared to bulk CMOS technology. The simulation results of 16 nm FinFet based inverter and CMOS TMC 0.13µm based inverter are presented. The PTM-CMG parameters are listed in table 1. The supply voltage (Vdd) is 0.9v and the input to inverters is pulse (0 0.9 3ns 0.5ns 0.5ns 14ns 20ns). The average power and measured propagation delay for these inverter circuits are listed in table 3.

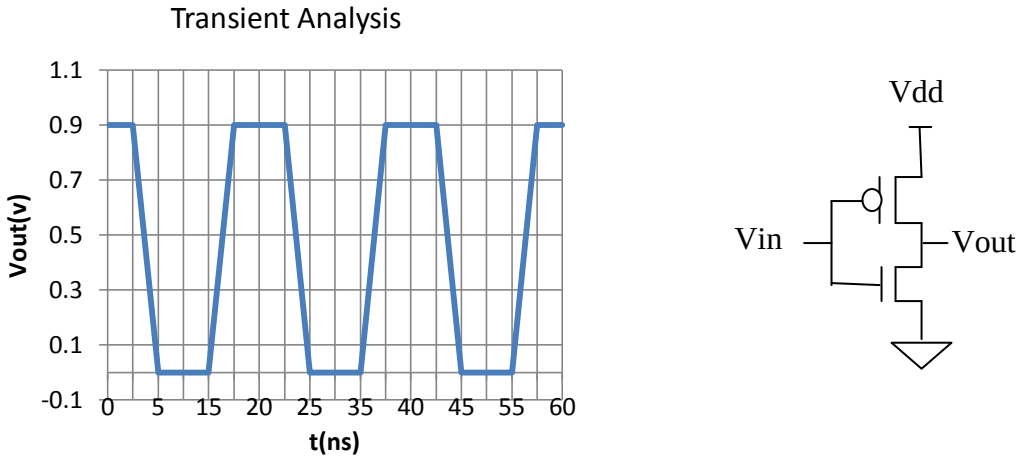

Figure 5 Transient analysis of CMOS based inverter and its circuit diagram

3.1 CMOS based inverter

The circuit diagram and input/output characteristics of CMOS 0.13 µm based inverter is shown in Figure 5.

3.2 FinFet based inverter

The circuit diagram of FinFet based inverter for the available technology configurations are shown in Fig6. These configurations are short-gate (SG) mode, low-power (LP) mode, independent-gate (IG) mode, and hybrid (IG/LP) mode. The dimensions are labeled using the corresponding BSIM-CMG model parameters. The 16 nm PTM model is used [2][3]. The transient outputs of these

configurations are investigated. The average power and measured propagation delay of these inverter circuits are listed in table 2.

Tabel 1 PTM-CMG Parameters

Parameters	Value(nm)
Gate length (L)	20
Fin thickness (Tfin)	12
Fin hight (Hfin)	26
Fin Pitch (Fpitch)	42
Equivalent oxide thickness (Eot)	0.8
Gate hight (Tgate)	9

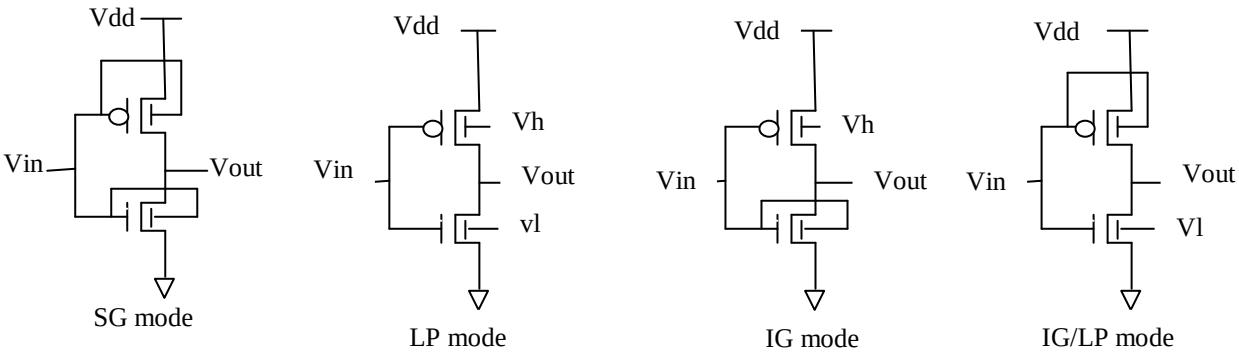

Figure 6 FinFet based inverter circuits

Table 2 FinFet based inverter performance

Technology	Average power (µw)	Delay(PS)
CMOS	0.39	20.1
FinFet SG	0.71	4.1
FinFet LP	0.35	4.5
FinFet IG	0.43	4.3
FinFet IG/LP	0.32	4.4

IV. TRANSCONDUCTANCE CIRCUIT TOPOLOGY AND DESIGN

The transconductance amplifier is a versatile voltage –controlled device designed for wide-bandwidth systems, including high performance video, RF and IF circuitry. It generates an output current that is a function of the differential input voltage. The FinFet transconductance circuit structure shown in Figure 7 is very popular among researchers for realization of low-power filter applications [4].

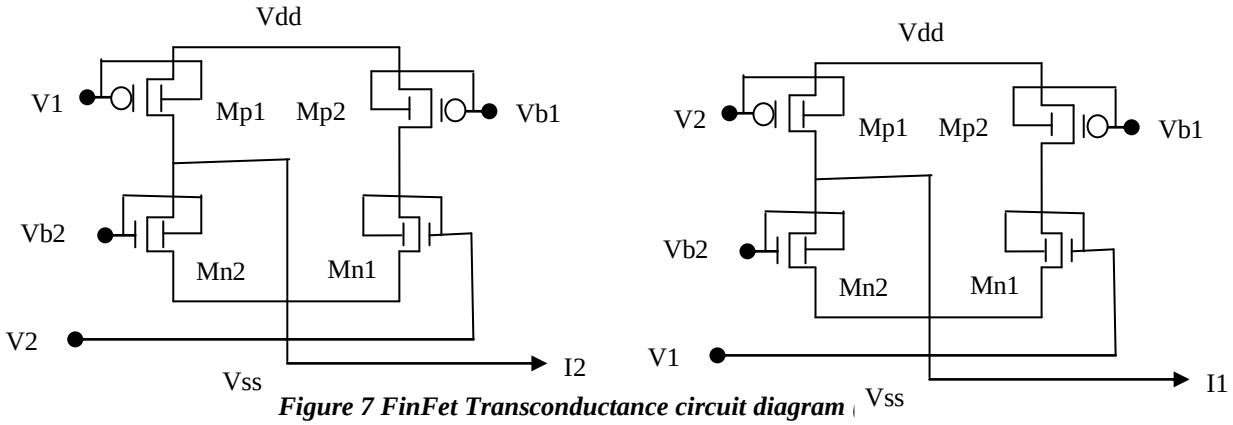

Figure 7 FinFet Transconductance circuit diagram

The small-signal model ignoring channel modulation effect [5] simplifying the transconductance to the following equation:

$$g_m = 2\left(g_{M_{p1}} - g_{M_{n1}}\right) \quad (4)$$

The proposed FinFet design is suitable for low power and wide frequency applications such as filter circuits. Vb1 and Vb2 are used to adjust the DC stability of the circuit and to assure that no residual dc current at the output nodes and zero differential transconductance.

The frequency limitations of this circuit will be determined by measuring the frequency response of the individual FinFet transistors which will be investigated in the next section.

4.1 Transimpedance Circuit Architecture

The proposed transimpedance circuit architecture according to the theory of feedback circuit is proposed as shown in Figure 8 [6][7]. The opposite directions of the voltage-controlled current-sources are obtained crossing the wires at the output of one transconductance.

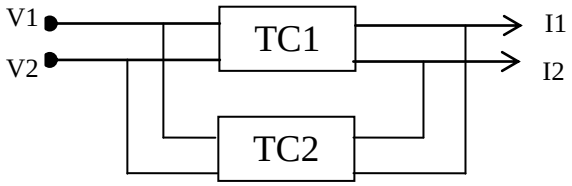

Figure 8 Transimpedance architecture

4.2 Voltage-mode filter architectures

The voltage-mode filter architectures are composed of transconductance (TC) and transimpedance (TI) blocks. The voltage-mode band-pass filter architecture is shown in figure 10. The value of the two capacitors can be varied to obtain different bandwidths and center frequencies. The voltage-mode low-pass filter architecture is shown in Figure 9. The capacitor c can be replaced by miller effect to adjust the frequency response of the filters. The voltage-mode low-pass filter response is shown in Figure 11 for 0.5 pF. The design of filters in high frequency band using FinFet technology has been considered in this paper [8][9]. The key blocks performances determine the overall system performance.

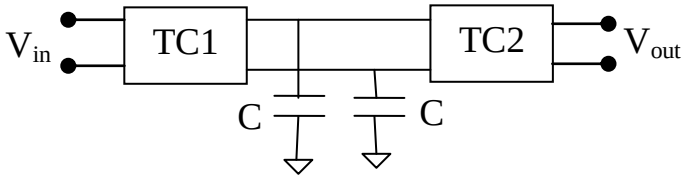

Figure 9 Voltage-mode low-pass filter architecture (LPF)

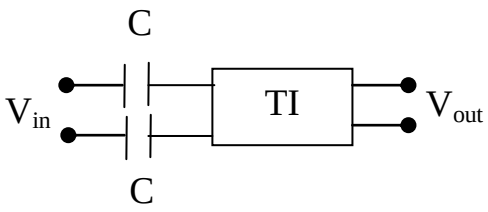

Figure 10 Voltage-mode Band-Pass filter architecture (BPF)

V. CONCLUSION

FinFet circuits are alternative for bulk CMOS circuits due to its ability to technology scaling requirements. They achieve lower functional voltage supply and low energy consumption compared to standard CMOS technology. The analysis and simulation of FinFet-based inverters configurations

verify minimum propagation delay compared to standard CMOS technology. The proposed voltage-mode FinFet transconductance and transimpedance blocks performance compatible with the low-voltage requirements of standard digital process. AS FinFet technology invented to work at GHz frequency range, RF circuit modeling and design will be new promising challenges in the future.

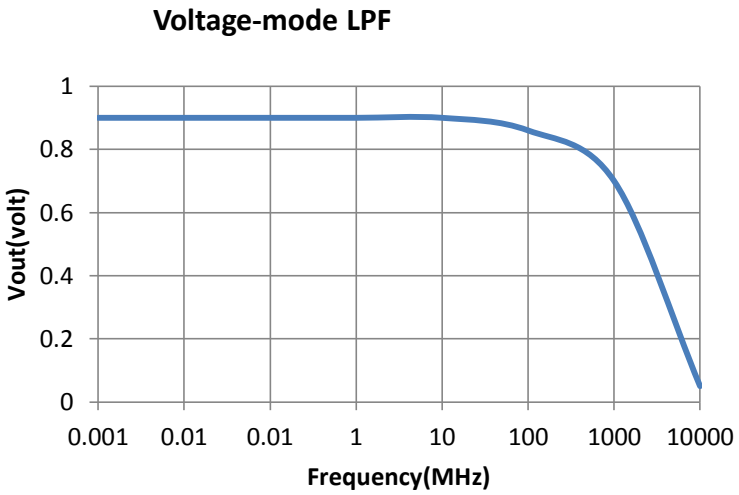

Figure 11 voltage-mode Low-Pass filter frequency Response

The advantages of FinFet technology arise since these devices can operates in the sub-threshold region with larger transconductance-to-current ratio than traditional Fets.

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