Design of router with priority scheduled arbiter for network on chip

Mrs. GOPIKA V
Assistant Professor, PPG Institute of Technology, Coimbatore.

Abstract - The System on Chip is an integrated circuit in which all the components of a computer or an electronic circuit can be integrated together. Network on Chip is a new method used for on chip communication which vanishes some of the problems faced by System on Chip. NoC consists of nodes and links and node to node communication happens through links. Data congestion occurs while large amount of data is getting transferred from node to node. Various routing algorithms are used to avoid data congestion. The bus arbiter is a device used to select which bus master is allowed to control the bus during a particular bus cycle. Based on the priority the input ports are allowed to transfer data to the output ports. A round robin arbiter is designed for NoC in this paper.

Key words- Network on Chip, System on Chip, Arbiter, Node to Node communication.

I. INTRODUCTION

Network on Chip is a new communication concept that overcomes the limitations of bus based architecture and satisfies all the requirements of future System on Chips. In NoC the routers connect the processing elements (PEs) like FPGA, ASIC and IP cores and the data is transferred from PEs through on-chip network. Therefore router is the most important component of NoC. The design and implementation of an efficient router depends upon an efficient arbiter that synchronizes the input and output ports based on a good scheduling mechanism.

An arbiter can determine the routing paths between the input and output ports and implements it so as to avoid data congestion. The design of arbiter should guarantee good scheduling, avoid starvation and provide high throughput. Multiple packets from different input ports compete for the same output port, therefore the switches of NoC must provide a high speed and cost effective scheduling technique to transfer the packets to output ports. A fast arbiter is a very dominant factor in NoC switches and the performance analyses of arbiters is very important in the design of NoC. In this paper a fast and fairness arbiter is designed to maximize the switch throughput and timing performance of Network on Chip.

II. ROUTER IN NoC

![Fig.1. Block diagram of router with arbiter](image-url)
The router is a networking device which forwards data packets between networks. It is the heart of the NoC as it performs the task of coordinating the data flow. The router mainly consists of a buffer, an arbiter and a crossbar. Whenever a packet is sending from one node to another the corresponding packet is stored in the input buffer. The control logic in the router will make the routing decision. After the decision is being made arbitration is done and the packet will be passed from the buffer to the crossbar and to the decided output port. The same process is repeated until the packet reaches the destination.

### III. ARBITER

Arbiter controls the flow of data between the ports and resolves contention problems. The status of communication happening between the ports is available in the arbiter and it knows which ports are free and which are communicating with each other. The packets having same priority and which are to be send to same output ports are scheduled by means of round robin arbiter. The arbiter will release the output port only when the last packet has finished transmission. The waiting packets can use the output port by the further arbitration of the arbiter. In this paper a round robin arbitration algorithm is used to assign priorities when more than one input ports want to transmit data to one output port. The crossbar will select the output port based on the output signal from the arbiter. The external clock signal high will indicate that data is now available on the output port of the source router. Read signal is generated if the FIFO is empty at that time. If the read signal is low it means that the FIFO buffer is not empty. Arbiter will generate three bit select line to select the output port.

![Arbiter – Input and Output lines](image)

### IV. ARBITRATION

The router proposed in this paper has five input ports (A to E) and five output ports (A to E). The packets with same priority destined to same output port are scheduled using round robin arbiter to avoid congestion. Consider the ports A, B, C, and D has to transfer packets with same priority to port E, a network congestion will occur if all the packets are transferred at the same time. To avoid this round robin arbitration is done.

![Arbitration of ports](image)
In round robin arbitration, the packets from port A are first transferred to port E. The packets from port B are transferred to port C and then from port C to port D and from port D to output port E. By the time the packets from port B arrive output port E, the packets from port A would have finished transmission so that the congestion of packets will not happen. The packets from input port travel in a round robin manner to the output port. A request which has just served will have low priority in next round of arbitration. The arbiter generates select lines for crossbar and reads or writes FIFO buffers based on the control logic.

V. RESULTS

The proposed design is developed using VHDL and simulated using XILINX 13.2. The main advantage of proposed arbiter is that the packets are transferred based on priority and the congestion of network is avoided when more than one input port is requesting the same output port.

Without congestion:

<table>
<thead>
<tr>
<th>SL NO</th>
<th>I/P PORT</th>
<th>SOURCE ADDRESS</th>
<th>DESTINATION ADDRESS</th>
<th>SELECT LINE</th>
<th>O/P PORT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Port A</td>
<td>000</td>
<td>001</td>
<td>Selb (000)</td>
<td>Port B</td>
</tr>
<tr>
<td>2</td>
<td>Port B</td>
<td>001</td>
<td>010</td>
<td>Selc (001)</td>
<td>Port C</td>
</tr>
<tr>
<td>3</td>
<td>Port C</td>
<td>010</td>
<td>011</td>
<td>Seld (010)</td>
<td>Port D</td>
</tr>
<tr>
<td>4</td>
<td>Port D</td>
<td>011</td>
<td>100</td>
<td>Sele (011)</td>
<td>Port E</td>
</tr>
<tr>
<td>5</td>
<td>Port E</td>
<td>100</td>
<td>000</td>
<td>Sela (100)</td>
<td>Port A</td>
</tr>
</tbody>
</table>

With congestion:

<table>
<thead>
<tr>
<th>SL NO</th>
<th>I/P PORT</th>
<th>SOURCE ADDRESS</th>
<th>DESTINATION ADDRESS</th>
<th>SELECT LINE</th>
<th>O/P PORT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Port A</td>
<td>000</td>
<td>100</td>
<td>Sele (000)</td>
<td>Port E</td>
</tr>
<tr>
<td>2</td>
<td>Port B</td>
<td>001</td>
<td>100</td>
<td>Sele (001)</td>
<td>Port E</td>
</tr>
<tr>
<td>3</td>
<td>Port C</td>
<td>010</td>
<td>100</td>
<td>Sele (010)</td>
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<td>100</td>
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<td>Port E</td>
<td>100</td>
<td>100</td>
<td>Sele (100)</td>
<td>Port E</td>
</tr>
</tbody>
</table>

![Fig.4. Simulation result without congestion](image-url)
VI. CONCLUSION

In this paper we have presented a new arbitration scheme aimed at reducing congestion in the links of NoC. The proposed scheme guarantees that all input requests are treated fairly. This kind of round robin arbitration method is suitable for all routers in NoC. The proposed scheme improves the data transfer speed to a great extend. The routing algorithm allows the transfer of data based on priority. Further the usage of arbiter serves the data from not getting lost.

REFERENCES


BIOGRAPHY

Gopika V received the BE degree from the Department of Electronics and Communication Engineering in Park College of Engineering and Technology (Anna University) Coimbatore, India in 2009 and ME degree from the Department of Electronics and Communication Engineering in Karpagam University, Coimbatore, India in 2015. She is currently working as Assistant Professor in the Department of Mechatronics with PPG Institute of Technology (Anna University), Coimbatore, India. Her research interests include wireless networks and robotics.