Design of Voltage Controlled Oscillator using Cadence tool

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Abstract- This paper presents the design of voltage controlled oscillator (VCO) based on ring oscillator. The VCO is designed for a frequency synthesizer module that generates local oscillation (LO) frequencies over a large bandwidth, targeting a multi-band acquisition system. The goal is a wide operating frequency tuning range of 500MHz – 5GHz in the VCO with low power consumption, -143 dBc/Hz@500MHz phase-noise performance and a good linearity for the frequency and control voltage characteristics. Simulation results verify the theoretical development and measurement results validate the design.

Keywords- Cadence; Virtuoso; Noise Margin; 180 nm technology; Voltage-Controlled Oscillator (VCO).

I.   INTRODUCTION

One of the key blocks in a communication system is the frequency synthesizer which is done mostly by using phase-locked loop (PLL) systems. A PLL system is composed of a phase detector, low pass filter and a voltage controlled oscillator as in Fig. 1.
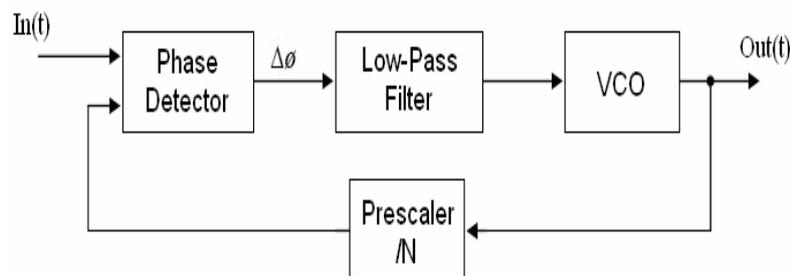

Fig 1. A typical PLL system

The action of the feedback in the loop causes the output frequency to be N times the reference input frequency of In(t) , usually a very stable, lower-frequency crystal oscillator. The spectral purity of the synthesized signal will largely depend on the quality of the VCO signal [1]. In actual communication systems there is a clear trend towards the full integration of the system into a single die for reasons of low cost and power consumption [2]-[4]. Since most of the CMOS transceivers incorporate the VCO active circuitry on the die, they are designed in a frequency range for which an external LC tank is avoided.On the other hand, large time constants required for the loop filter generally lead to large external capacitors. As an alternative, a ring oscillator

can be integrated in a standard CMOS process without any extra processing steps because it does not require any passive resonant element. In addition, when the ring oscillator is employed for a VCO the desired wide operating-frequency range can be easily obtained but with the drawback of poorer phase-noise performance than the LC tank oscillator because of its low effective quality factor [5].
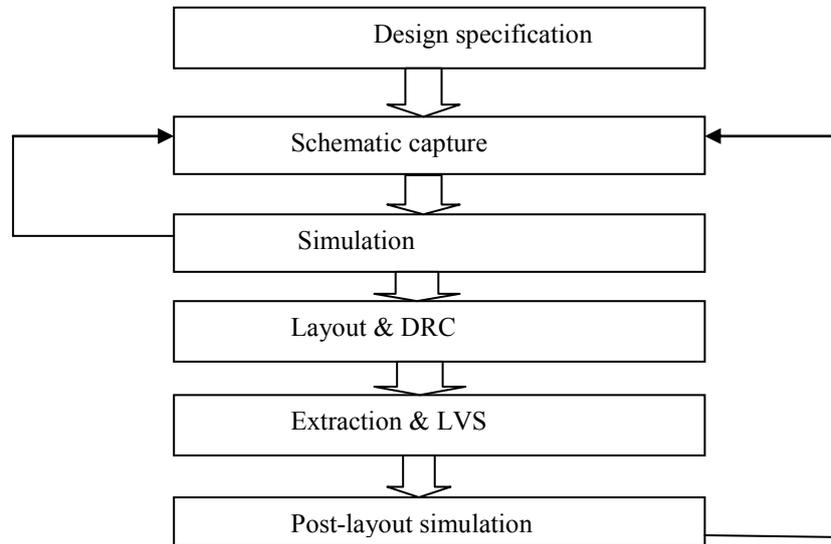

Fig 2. Cadence flow

II.   CIRCUIT DESCRIPTION

Ring oscillator is cascaded combination of delay stages, connected in a close loop chain [6]. The ring oscillator designed with a chain of delay stages has created great interest because of their numerous useful features. These attractive features are: (i) It can achieve its oscillations at low voltage, (ii) It can be easily designed with the state-of-art integrated circuit technology (CMOS, BiCMOS), (iii) It can be electrically tuned, (v) It can provide wide tuning range, (iv) It can provide high- frequency oscillations with dissipating low power, and (vi) It can provide multiphase outputs because of their basic structure [7]. To increase the frequency of oscillation, two methods are commonly used. Firstly, the applied voltage may be increased. Secondly, making the ring from a smaller number of inverters results in a higher frequency of oscillation given certain power consumption.

The VCO consist of three stage inverter which is designed by using one NMOS and one PMOS transistor. PMOS transistor work as pull-up network and NMOS transistor is connected to pull down network. One more NMOS connecting to each of inverter with Vbias, In this combination, PMOS transistor connected to power supply and NMOS transistor connected to be ground. Inverter schematic & it's working region given as

$$I_D = 0 \qquad (\text{off} \ |V_{GS}| < |V_{TH}|) \tag{1}$$

$$I_D = \mu.C_{OX}*W/L[(V_{GS} - V_{TH})V_{DS} - V^2_{DS}/2] \ (\text{triode:} \ |V_{DS}| < |V_{GS}| - |V_{TH}|) \tag{2}$$

$$I_D = \mu.C_{OX}*W/2L \ (V_{GS} - V_{TH})^2 \qquad (\text{Saturation:} \ V_{DS} \geq V_{GS} - V_{TH}) \tag{3}$$
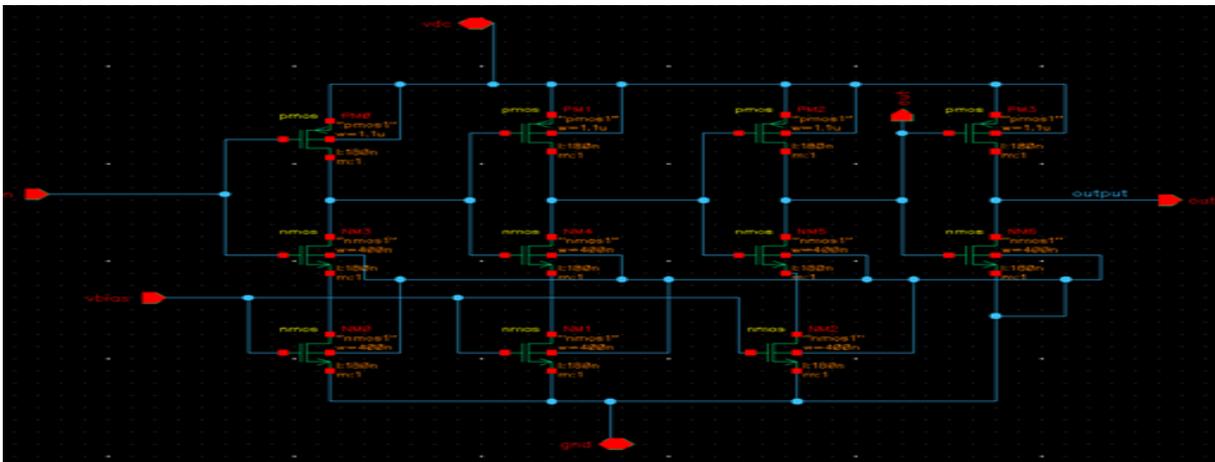
Fig 3. Schematic of VCO

III. DESIGN METHODOLOGY

3.1. Running the Cadence tools

We should be able to run the Cadence tools. Never run Cadence from your root directory, it creates many extra files that will clutter your root. Instead please create a directory (e.g. cadence) and start Cadence there by typing:

```
#Mkdir cadence
# cd cadence
# icfb &
```
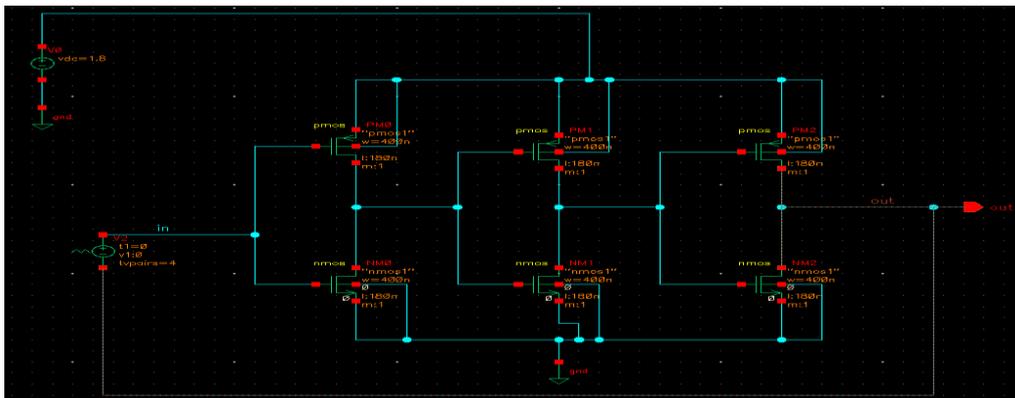
3.2. Schematic capture

Fig 4. Schematic diag. of Ring oscillator using cadence tool.

The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. Also included in the schematic are the power supply and ground connections as well as all "pins" for the input and output signals of your circuit. This information is crucial for generating the corresponding netlist which is used in later stages of the design. The generation of a complete circuit schematic is therefore the first important step of the design flow.

IV.   SIMULATION AND MEASUREMENT RESULTS

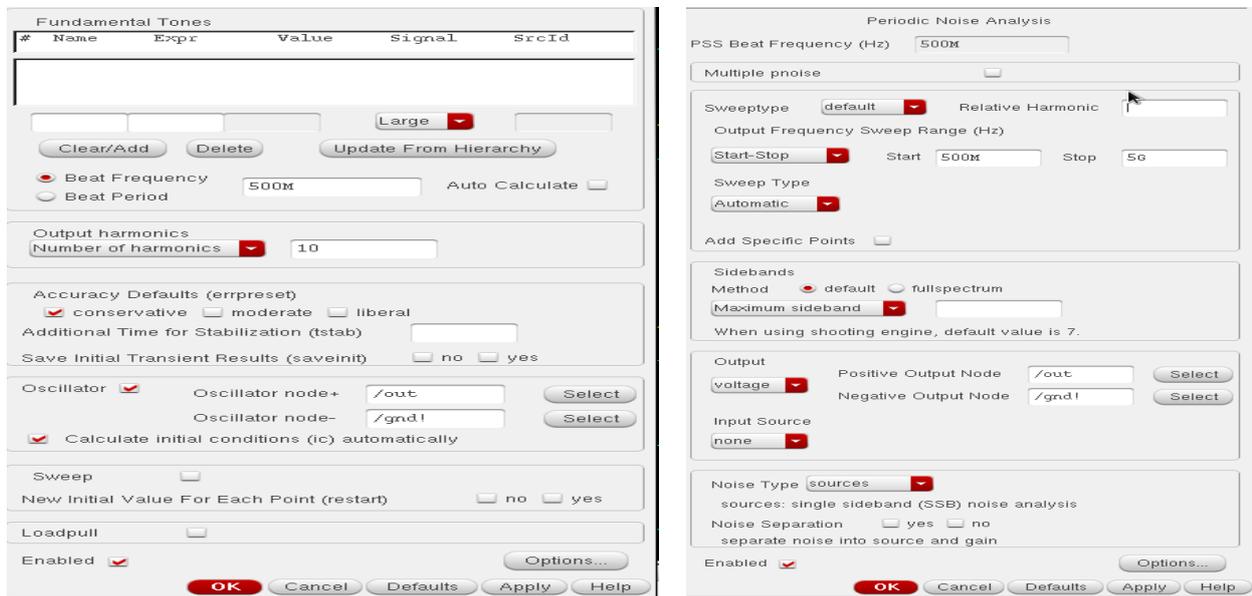### 4.1. Pss and pnoise analysis

Fig 5. Chosing pss and pnoise analysis

Periodic Steady-State (PSS) analysis is a large-signal analysis that directly computes the periodic steady-state response of a circuit With PSS simulation times are independent of time constants of the circuit, so pss can quickly compute the steady state response of the circuit with long time. Periodic Noise analysis (Pnoise) are similar tothe Spectre AC, SP, XF, and Noise analyses, but we can apply them to periodically drivencircuits that exhibit frequency conversion.
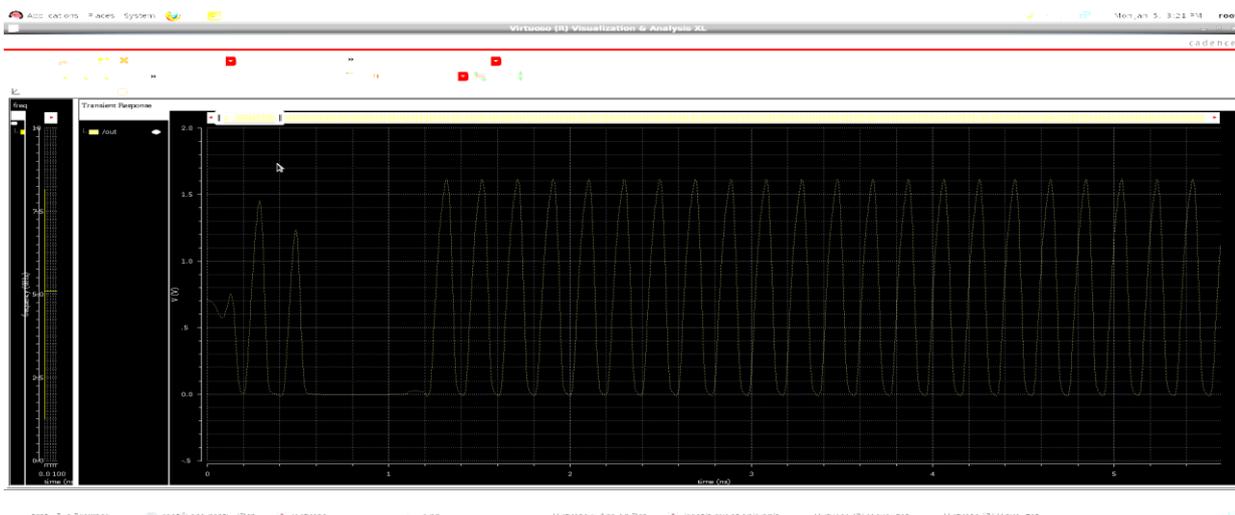
4.2.Transient response

Fig 6. Transient response(ns)
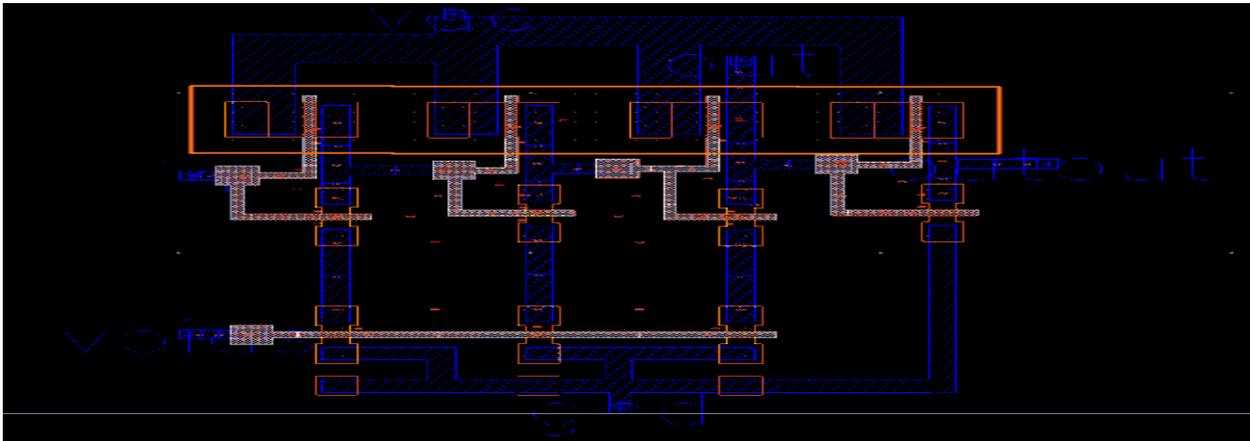
4.3.VCO Layout

Fig 7. Proposed VCO Layout

CONCLUSIONS

Ring oscillators are basic building blocks of complex intergrated circuit. They are mainly used as clock generating circuits. Many different types of ring oscillators are presented in literatues[8-9]. They differ in respect to architechtural, realisiation of inverter stages. In this paper we have considered realisation of ring oscillator based on four different types of single-ended inverters. The simulation was performed using Cadence virtuoso spectre rhel 6.1 version and library model is 180gpdk CMOS techonoly.

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