International Journal of Modern Trends in Engineering and Research
www.ijmter.com
e-ISSN No.:2349-9745, Date: 2-4 July, 2015

Design a Full Adder Block for optimization of PDP

Neha K. Sancheti[1] , Shubhangi S. Bachhav[2]

[1]*Department of E&TC Engg., SNJB's KBJ COE, Chandwad(MH),India*
[2]*Department of E&TC Engg., SNJB's KBJ COE, Chandwad, Nasik (MH)India*

Abstract- In early days the explosive growth in laptops, portable personal communication systems and the evolution of the lessening technology, the research effort in low-power microelectronics has been intensified and low-power VLSI systems have emerged as highly in demand. An adder is a critical component in systems like processor, memory design, arithmetic logic unit etc. Therefore careful design of these circuits improves the power consumption and other performance metrics of VLSI systems. The purpose of this work is to study the impact of different full adder cells layout in MICROWIND tool at 45nm technology. For analysis CMOS conventional 28T full adder and CMOS 24T mirror based full adders layout is implemented. For comparison the parameters like power dissipation, area, delay and PDP are used.

Keywords- Full adder, Power Dissipation, ALU, PDP, Layout.

I. INTRODUCTION

Now a day's power is the primary troubled due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption change application to application. Finally for the high performance non battery operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability. For such high performance systems, process technology has driven power to the fore front to all factors in such designs. At process nodes below 100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques [1] that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance [2].Addition is very basic operation in arithmetic, Subtraction, multiplication, division and address calculation are some of the well-known operation based on addition. These operation are used in many VLSI application such as in DSP processor for convolution, correlation etc., since full adder cell is the building block of the binary adder, enhancing the performance of the 1 bit full adder is significant goal and has attracted much attention.

Many full adders have been designed and published. They are built upon different logic styles. Among these adders the circuit explained below will be used for comparisons. Although all of them perform a similar function, but the method of producing the intermediate nodes and the outputs, the loads on them and transistor count are varied. Different logic styles tend to favor one performance aspect at the expense of the other. Some of them use more than one logic style for their

@IJMTER-2015, All rights Reserved

implementation. In all of these full adders, it is tried to reduce power and delay factor and thus decrease power-delay-product (PDP) in comparison. In the following a brief description of each full adder is presented. The most conventional one is complementary CMOS-full adder(C-CMOS)[3]. It is based on regular CMOS structure with pull up and pull-down transistor and has 28 transistors. Another conventional adder is the complementary Pass transistor logic (CPL)[3] with swing restoration which uses 32 transistors .CPL produces many intermediate nodes and their complement to make the outputs. The basic difference between the pass-transistor logic and complementary CMOS logic style is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines [3]. In Majority based Bridge style full adder [4].The designs is that the Cout function is the same as 3-input majority function. It was design majority gates with more inputs by this method by increasing the number of input capacitors. The capacitor network is used to supply voltage division for implementing majority logic. Using the bridge circuit leads to reduction of delay and power consumption of the Full Adder cell and also increases the robustness and reliability of the circuit. In Minority based Bridge style full adder [5]. In this the Cout function can be implemented by a Minority circuit and the Sum function can be implemented using Cout.

II. POWER DISSIPATION FACTOR

In a circuit three components are responsible for power dissipation:

1. Dynamic power,
2. Short-circuit power and
3. Static power.

Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below [5, 6]:

$$P_{dyn}=C_L V_{DD}^2 f\alpha \qquad (1)$$

CL: Load Capacitance, a function of fan-out, wire length, and transistor size,
VDD: Supply Voltage, which has been dropping with successive process nodes,
α: Activity Factor, meaning how often, on average, the wires switch,
fclk: Clock Frequency, which is increasing at each successive process node.

III. FULL ADDER

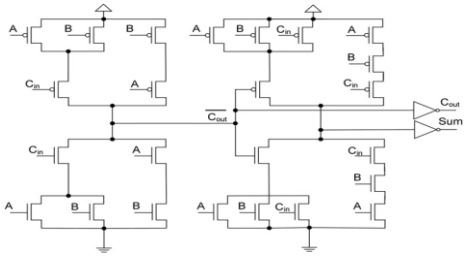

Figure 1. Typical 28-transistor mirror FA

Figure 1 shows the typical 28-transistor mirror FA. The carry is generated first since it is on the critical path, and then it is reused in the sum generation to obtain low area. Conventional CMOS [10] full adder in Figure 1 with 28 transistors is a robust, high power and area full adder, which has been designed, based on standard CMOS topology. It has full-swing outputs that increase noise margin and

@IJMTER-2015, All rights Reserved

reliability. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result the high input capacitances, which cause high delay and dynamic power. However, using inverters on the output nodes decreases the rise-time and fall-time and increases the driving ability. It functions well at low power supply voltages because it does not have reducing threshold loss problem.

$$SUM = \overline{Cout}A + \overline{Cout}B + \overline{Cout}Cin + ABCin \quad (2)$$

$$C_{out} = (A+B)C_{in} + AB \quad (3)$$

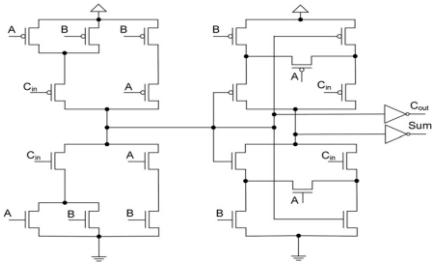

Figure 2. 24T FA Mirror Based Full Adder

The mirror FA that consists of 24 transistors is shown in Figure 2. Compared to the previous FA, the transistor count is reduced for the sum generation while the circuitry for the carry generation is the same as in Figure 1 This full adder is nothing but the mixture of complimentary and pass transistor. The carry generation circuitry is designed by complementary transistor which output of this circuitry is COUT-. Next circuitry is connected to Cout for sum operation which design by pass transistor logic and dynamic logic. Full adder is implemented the same Boolean function, which is given in Equation 2 and 3.

III. IMPLEMENTED FULL ADDER

The layout of 28T full adder and 24T full adder designed in Microwind simulator at 45nm technology. For drawing the layout firstly we draw the stick diagram of 28T full adder circuit and 24T full adder circuit on paper. By reference of stick diagram draw the layout, we generate the PMOS transistor which has W/L as 0.20/0.04 by default generated by tool. As per the structure we generate 3 or 4 combine PMOS transistor. Generate the NMOS transistor which has W/L as 0.20/0.04 by default generated by tool. As per requirement we generate the PMOS and NMOS transistor. As per the circuit diagram, connect all terminals by Metal 1 layer. But at some connection the Metal 1 layer has overlapped that time we used the Metal 2 layer. For see the internal connection we see their 3D view, in that we had observed that all interconnection of Metal 1 with poly-silicon or Metal 1 with Metal 2. Also we connect all gate terminals, for short distance poly-silicon used but for large distance we used Metal 1 layer also because poly-silicon metal has high capacitance which increase dynamic power dissipation.

Whenever we complete this layout then simulate it then we can observe that it has high power dissipation up to 22.2uW and area is also 32um2. After that we reduced the W/L of transistor 0.08/0.02 um and all PMOS transistor was designed in one n-well. The n-well of all PMOS transistor is common so we had applied the common Vddto n-Well. Also to reduced their wire-length by

@IJMTER-2015, All rights Reserved

adjusting transistor position as per circuit given in layout.

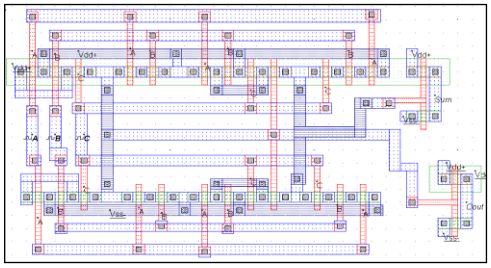

Figure 3. optimize layout of 28T full adder

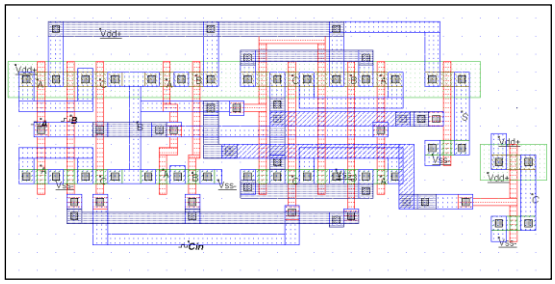

Figure 4. optimize layout of 24T full addder

Design the optimize layout of 24T full Adder and 24T full Adder. Apply different input clock frequencies for analysis of maximum input speed of full Adder. Also apply different power supply for study their performance .The optimize layout of 28T and 24T full adder respectively as shown in fig 3 and fig 4.

IV. RESULTS AND DISCUSSION

The two full adders: conventional 28T full adder and 24T full adder are all simulated using 0.45nm CMOS process. The threshold voltage of the NMOS and PMOS transistors are around 0.22and 0.32V, the supply voltage is 1V and the frequency (clock rate) is 800 Mhz. Microwind 3.2 circuit simulator is used for simulation. The layout of 28T full adder and 24T full adder are shown in Figure 3 & 4.

All of the circuits are sized appropriately to minimize the PDP metric using an improved version of the algorithm. The designs are simulated at different supply voltage and with the aim of reaching the optimum PDP. Complete input pattern containing all the 64 possible transitions from an input combination to another is applied to the circuit for measuring the propagation delay. The propagation delay of each adder cell is measured from the moment that the input signal reaches 1/2Vdd to the moment that the output signal reaches the same voltage level.

Table1. Comparison of different parameters

Parameter	Voltage Ranges							
	0.8V		**0.9V**		**1V**		**1.1V**	
	28T	*24T*	*28T*	*24T*	*28T*	*24T*	*28T*	*24T*
PD(uW)	0.135	0.142	0.163	0.171	0.195	0.204	0.419	0.471
Delay C(ps)	49.7	44.62	45.16	40.2	40.7	36.8	38.7	34.8
Delay S (ps)	69.7	71.62	63.38	64.72	58.66	59.9	54.8	56.1
PDP (fJ)	0.081	0.083	0.088	0.089	0.097	0.099	0.191	0.214

@IJMTER-2015, All rights Reserved

All of the transitions from an input to another checked and the delay of each transition is evaluated and the maximum value is reported as the propagation delay of each adder. The average power consumption is also measured by applying a complete pattern during a long period of time. In order to make a trade-off between the delay and the power consumption parameters, the PDP metric is calculated, which is the multiplication of average power consumption and critical path delay. Therefore, this metric is could be useful for comparing the performance of the adder cell. Detail experimental results are listed in Table 1 and table 2. Comparison of full adders designed to achieve minimum PDP is discussed below, three subsections refer to DELAY, POWER and PDP.
In addition, the proposed layout result is compared with other full adder cell which is simulated at 45nm technology node at 1V. The simulation results, shown in Table 1, demonstrate the superiority of the proposed layout of 24T FA and 28T FA design in terms of delay, power dissipation and PDP.

Table 1. Simulation results of different parameter

Full Adders	**Parameter Measured**		
	Delay(nS)	Power Dissipation(uW)	PDP(fJ)
MBFA	1.513	0.681	0.103
MinFA	2.499	0.562	0.141
InvFA	3.643	1.154	0.421
BCFA	2.295	0.904	0.201
HCFA	2.715	0.635	0.172
Proposed Layout(28T FA)	**0.501**	**0.195**	**0.097**
Proposed Layout (24T FA)	**0.491**	**0.204**	**0.099**

Delay comparison:
The values of delay obtained for considered value of VDD (1V) for all full adders are shown in Table 2. It is apparent that full adders, conventional 28T full adder have the small Sum (ps) delay, as compared to 24T full adder. But the 28T full adder has the higher the Carry (ps) delay, as compared to 24T full adder. As we can see performance of the 24-transistor full adder circuit is better in comparison with new 28-transistor Full adder speed.

Power comparison:
Average power dissipation of all the full adders is shown in Table 1. The adder dissipates the most power because of its complementary structure and high number of internal nodes in its design. 24T full adder have lesser transistor count in comparison to 28T full adder, but due to the lack of drivability, additional buffers are required at each output, which increase their short circuit power as well as switching power. Among those full adders, 28T has the lowest power dissipation.

@IJMTER-2015, All rights Reserved

PDP comparison:

The PDP is a quantitative measure of the efficiency of the tradeoff between power dissipation and speed and is particularly important when low power operation is needed. The values of PDP, evaluated under 1 V supply voltage, are summarized in Table 1. As shown in Table 2, The28T has the better PDP in comparison with the 24T full adder. The PDP improvement of 28T full adder is 18% in comparison with 24T Full adder. As we can see the delay degradation in 28T is compensated with the improvement in its power dissipation, leading to a better PDP.

V. CONCLUSION

To design a layout of 28T full adder and 24T full adder at the 45nm technology in MICROWIND 3.5.Simulate this layout by applying different power supply 0.8V to 1.1V.The simulation result has been indicate the 28T full adder has lower power dissipation but more propagation delay as compared to 24T full adder. So the 28T full adder has lower PDP to 24T full adder. It used in portable application such as cell phone, laptop etc. Full adder used in digital signaling processing to execute complex algorithm such as convolution, correlation and digital filtering.ALU used in processor of computer. Future Scope is, we can implement 32bit ALU for 8 operation, we used this full adder in BCD adder etc.

REFERENCES

[1] Kanika kaur1,Aartinoor "Strategies & methodologies for low power VLSI designs"21kiit college OF engineering, gurgaon, INDIA INTERNATIONAL journal OF advances IN engineering & technology, may 2011. ©ijaetissn: 2231-1963

[2] Rahul. M.Rao, Jeffery L.Burns, Richard B.Brown, "Circuit Techniques for gate and subthreshold leakage minimization in future CMOS technologies" Proc. ISLPED, pp70-73, 2002.
A.M. Shams, T.K. Darwish, M.A. Bayoumi, Performance analysis of low-power 1-bit CMOS Full Adder cells, IEEE Transactions on VLSI Systems 10 (2002) 20–29.

[3] K. Navi, M.H. Moaiyeri, R. Faghih Mirzaee, O. Hashemipour, B. MazloomNezhad, Two new low-power full Adders based on majority-not gates, Microelectronics Journal, Elsevier 40 (2009) 126–130. [13]

[4] Keivan Navia,n, Horialsadat Hossein Sajedib, Reza Faghih Mirzaeec, Mohammad Hossein Moaiyeria, Ali Jalalia, OmidKaveheid "High-speed full adder based on minority function and bridge style for nanoscale" Microelectronics Journal, Elsevier 40 (2008) 111–120. [13]

[5] Mentor Graphics, "Low power physical design with Olympus SOC", Place and route white paper, March27, 2009

[6] M.Alidina, j. Monterio, S. Devadas, A.Ghosh and M. Papaefthymiou. "Precomputation –based Sequentiallogic optimization for low power" In Proceedings of the 1994 International Workshop on Low Power Design,pages 57-62, April 1994.

[7] De-ShiuanChiou, Shih-Hsin Chen, ChingweiYeh, "Timing driven power gating", Proceedings of the 43rdannual conference on Design automation,ACM Special Interest Group on Design Automation, pp.121 - 124,2006.

[8] Keivan Navia,n, Horialsadat Hossein Sajedib, Reza Faghih Mirzaeec, Mohammad Hossein Moaiyeria, Ali Jalalia, OmidKaveheid /'High-speed full adder based on minority function and bridge style for nanoscale.

@IJMTER-2015, All rights Reserved