Temperaments in the Design of Low-voltage Low-power Double Tail Comparator

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Abstract—The circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-μm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 μW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

Keywords—Double-tail comparator; Dynamic Clocked comparators; High-speed analog-to-digital comparators; Low power analog design

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep sub-micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [3]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [1], [2], techniques employing body-driven transistors [7], [8], current-mode design [5] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Here, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [5], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

II. DESIGN

Fig. 1 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control...
transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner.

During operation, in the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (CLK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about V_{DD}). Thus, f_n and f_p start to drop with different rates according to the input voltages. Suppose V_{INP} > V_{INN}, thus f_n drops faster than f_p, (since M_2 provides more current than M_1).

As long as f_n continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling f_p node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing f_n to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔV_{fn/fp} is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node f_n discharges faster, a pMOS transistor(M_{c1}) turns on, pulling the other node f_p back to the V_{DD}.
Therefore by the time passing, the difference between $f_n$ and $f_p$ ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., $M_{c1}$) turns on, a current from $V_{DD}$ is drawn to the ground via input and tail-transistor (e.g., $M_{c1}$, $M_1$, and $M_{tail1}$), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [$M_{sw1}$ and $M_{sw2}$, as shown in Fig. 2].

2.2 Delay Analysis
2.2.1 Enhancing $\Delta V_0$

We define $t_0$, as a time after which latch regeneration starts. In other words, $t_0$ is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. According to (2), the latch output voltage difference at time $t_0$, ($\Delta V_0$) has a considerable impact on the latch regeneration time, such that bigger $\Delta V_0$ results in less regeneration time.

2.2.2 Effects of enhancing latch effective transconductances

In conventional double-tail comparator, both $f_n$ and $f_p$ nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes ($f_n/f_p$) will charge up back to the $V_{DD}$ at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective.

2.2.3 Reducing the energy per comparison

It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. Earlier in conventional double-tail topology, both $f_n$ and $f_p$ nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the $V_{DD}$. However, in our proposed comparator, only one of the mentioned nodes ($f_n/f_p$) has to be charged during the reset phase.

1.3 Design Considerations

In designing the proposed comparator, some design issues must be considered. When determining the size of tail transistors ($M_{tail1}$ and $M_{tail2}$), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than $t_0$ (start of regeneration).

\[
\text{ton,} M_{c1}(2) \rightarrow \frac{|V_{Thp.CL}.f_n(p)|}{In_{1,2}} < \frac{V_{ThnCLout}}{IB1} \\
\rightarrow \frac{|V_{Thp.CL}.f_n(p)|}{Itail1} < \frac{V_{ThnCLout}}{\frac{Itail2}{2}}
\]

CONCLUSIONS

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.
REFERENCES


